

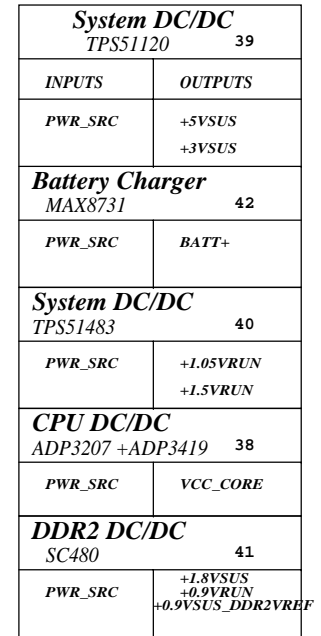
Vinafix

Project code: 91.1E201.001

PCB P/N : 05224

PCB REVISION:-1

DELL REVISION:A00



1208-1500



Title	
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System Block Diagram

Size	Document Number	Rev
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A3	Bermuda	-1
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ICH7M Functional Strap Definitions

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Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSPLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

Calistoga Strapping Signals and Configuration

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPIO17, PME#, LAD[3:0]#/FWH[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+0.25 Center
1	0	0	1	+0.5 Center
1	0	1	0	+0.75 Center
1	0	1	1	+1.0 Center
1	1	0	0	+0.25 Center
1	1	0	1	+0.5 Center
1	1	1	0	+0.75 Center
1	1	1	1	+1.0 Center


PCI Routing

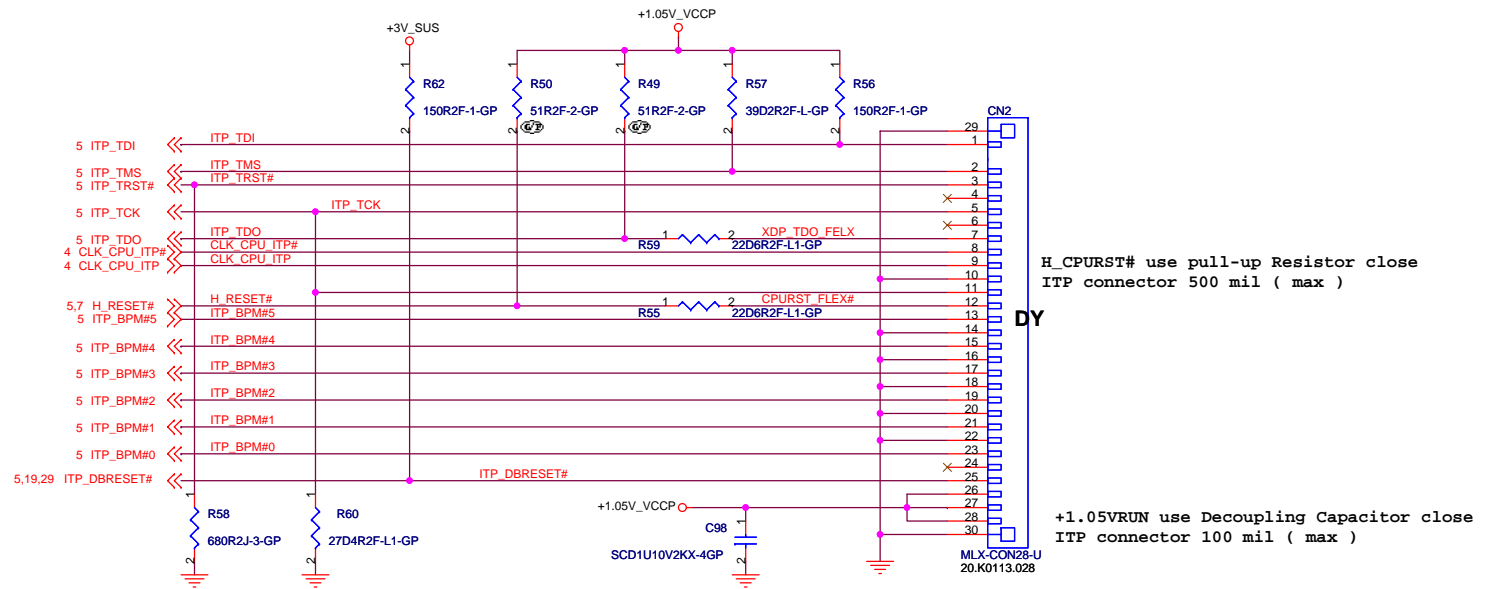
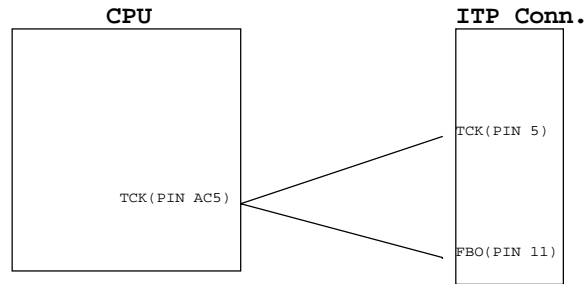
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	IDSEL	IRQ	REQ/GNT
R5C832	AD17		
LAN	AD16		

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Table of Content			
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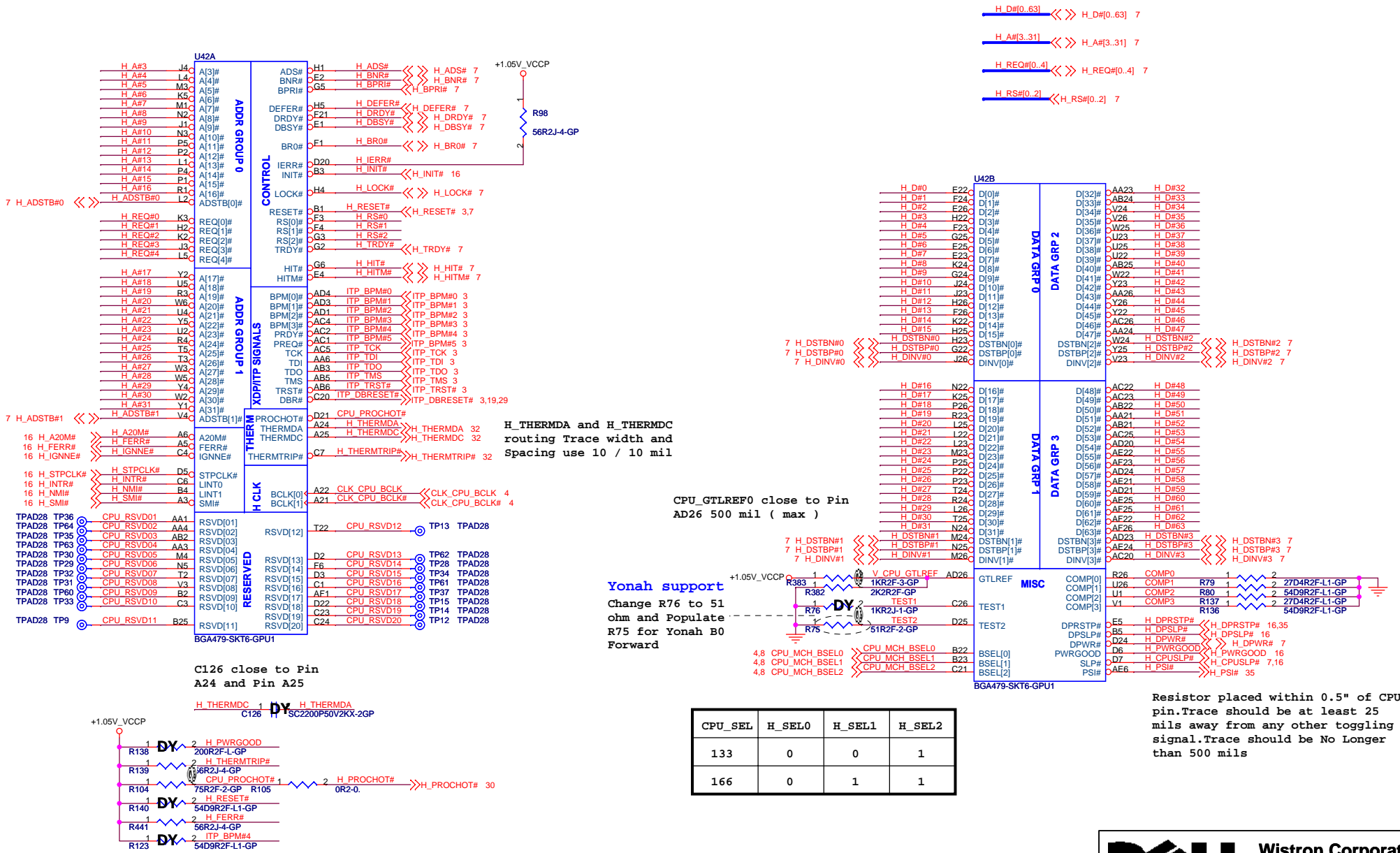


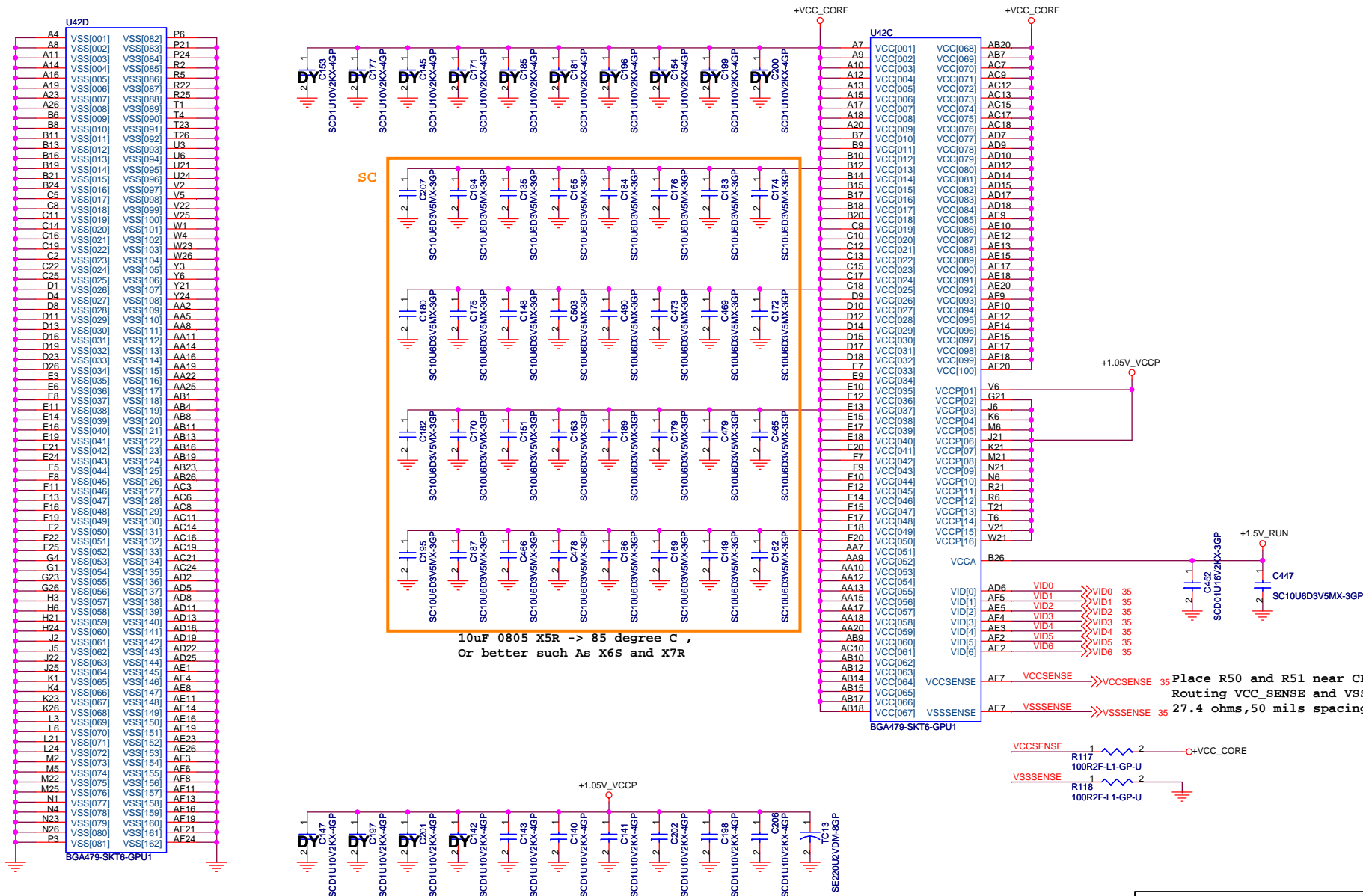
ITP Debug Conn.

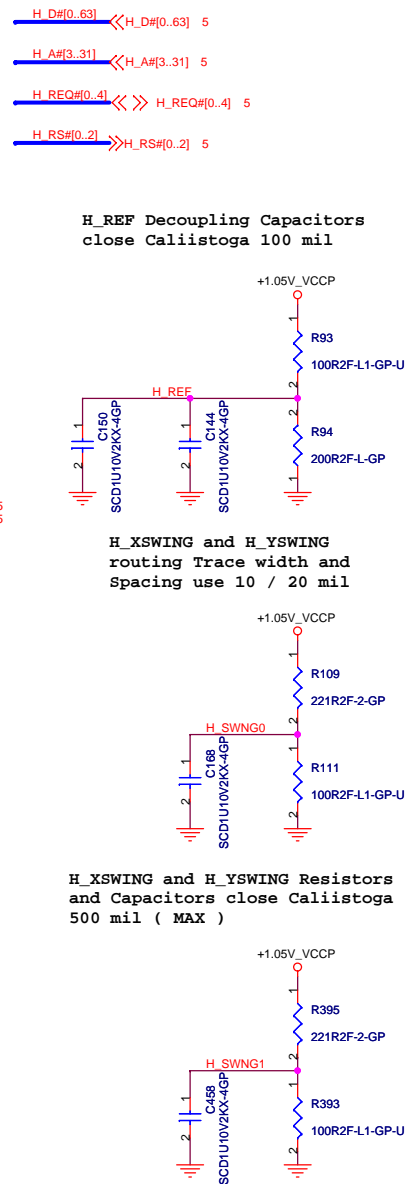
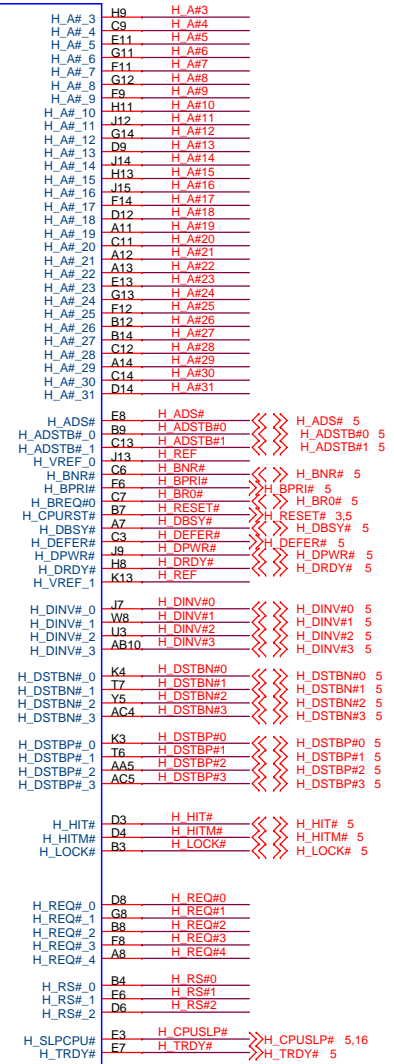
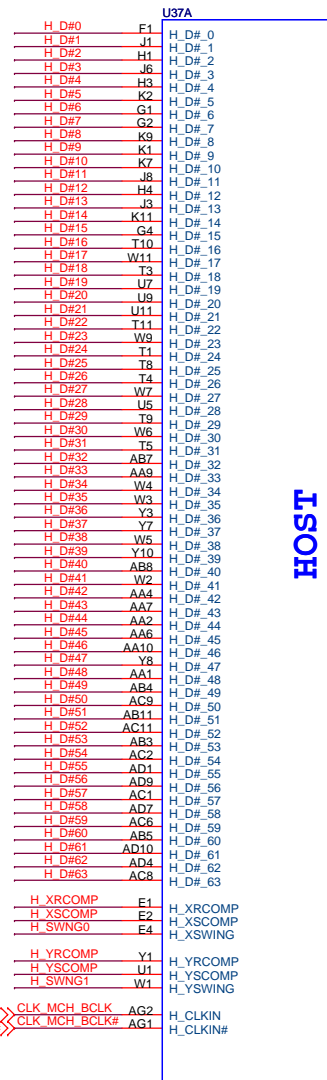
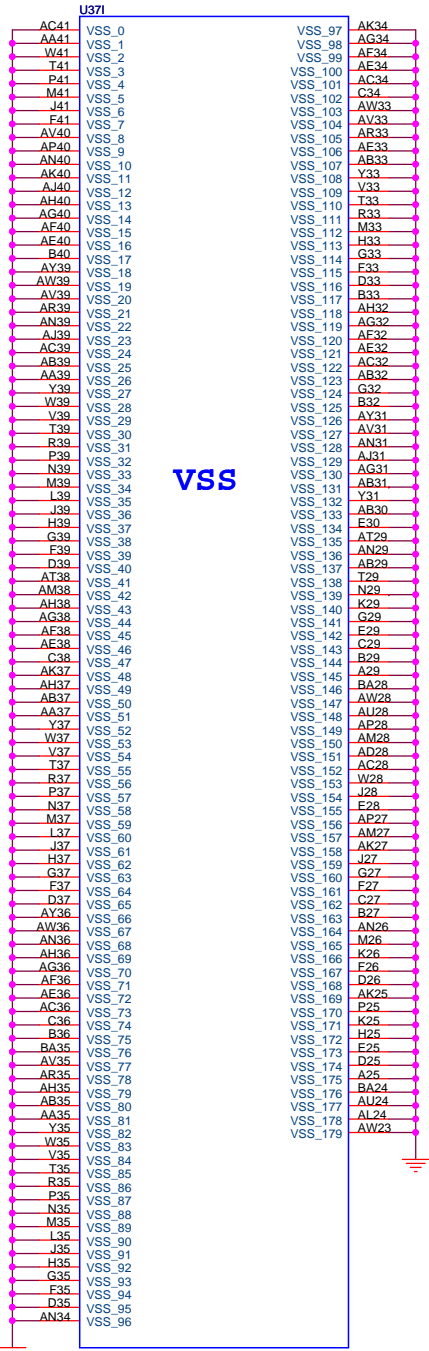
SEL2 SEL1 SEL0 CPU FSB

0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

Wistron Corporation
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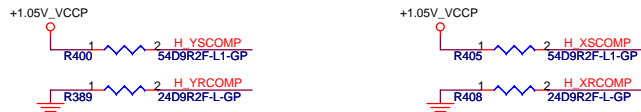


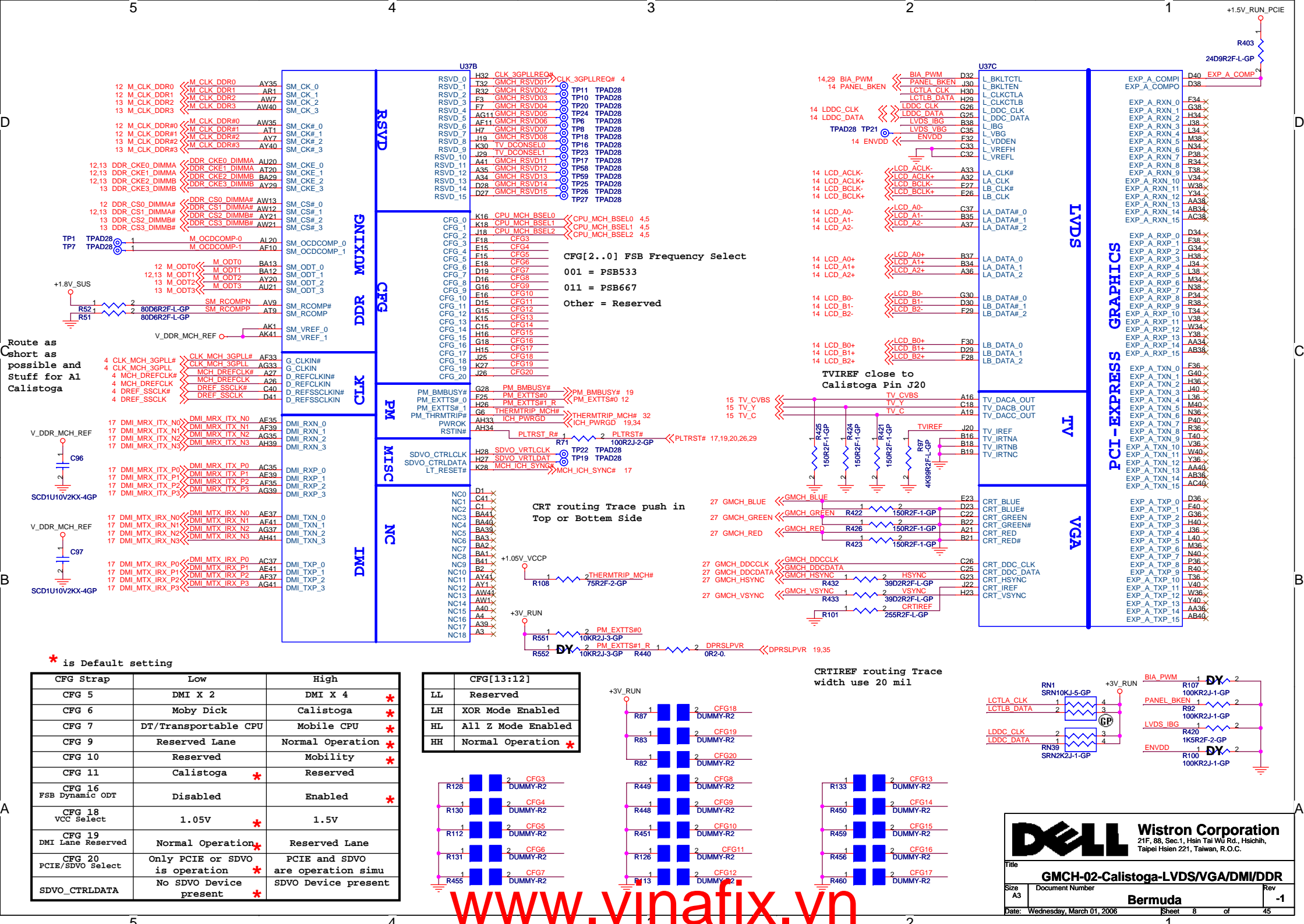




H_XRCOMP and H_YRCOMP routing Trace width and Spacing use 10 / 20 mil

H_XSCOMP and H_YSCOMP Resistors and Capacitors close Caliistoga 500 mil (MAX)





U37J		
AT23	VSS 180	VSS 273
AN23	VSS 181	VSS 274
AM23	VSS 182	VSS 275
AK23	VSS 183	VSS 276
AC23	VSS 184	VSS 277
W23	VSS 185	VSS 278
K23	VSS 186	VSS 279
J23	VSS 187	VSS 280
F23	VSS 188	VSS 281
G23	VSS 189	VSS 282
AA22	VSS 190	VSS 283
K22	VSS 191	VSS 284
G22	VSS 192	VSS 285
F22	VSS 193	VSS 286
E22	VSS 194	VSS 287
D22	VSS 195	VSS 288
BA21	VSS 196	VSS 289
AV21	VSS 197	VSS 290
AR21	VSS 198	VSS 291
AN21	VSS 199	VSS 292
AL21	VSS 200	VSS 293
AB21	VSS 201	VSS 294
Y21	VSS 202	VSS 295
P21	VSS 203	VSS 296
K21	VSS 204	VSS 297
J21	VSS 205	VSS 298
H21	VSS 206	VSS 299
C21	VSS 207	VSS 300
AW20	VSS 208	VSS 301
AR20	VSS 209	VSS 302
AM20	VSS 210	VSS 303
AA20	VSS 211	VSS 304
K20	VSS 212	VSS 305
B20	VSS 213	VSS 306
A20	VSS 214	VSS 307
AN19	VSS 215	VSS 308
AC19	VSS 216	VSS 309
W19	VSS 217	VSS 310
K19	VSS 218	VSS 311
G19	VSS 219	VSS 312
G19	VSS 220	VSS 313
C19	VSS 221	VSS 314
AH18	VSS 222	VSS 315
P18	VSS 223	VSS 316
H18	VSS 224	VSS 317
D18	VSS 225	VSS 318
A18	VSS 226	VSS 319
AY17	VSS 227	VSS 320
AR17	VSS 228	VSS 321
AP17	VSS 229	VSS 322
AM17	VSS 230	VSS 323
AK17	VSS 231	VSS 324
AV16	VSS 232	VSS 325
AN16	VSS 233	VSS 326
AL16	VSS 234	VSS 327
AB16	VSS 235	VSS 328
F16	VSS 236	VSS 329
C16	VSS 237	VSS 330
AM15	VSS 238	VSS 331
AM15	VSS 239	VSS 332
AK15	VSS 240	VSS 333
N15	VSS 241	VSS 334
M15	VSS 242	VSS 335
L15	VSS 243	VSS 336
B15	VSS 244	VSS 337
A15	VSS 245	VSS 338
BA14	VSS 246	VSS 339
AT14	VSS 247	VSS 340
AK14	VSS 248	VSS 341
AD14	VSS 249	VSS 342
AA14	VSS 250	VSS 343
U14	VSS 251	VSS 344
K14	VSS 252	VSS 345
H14	VSS 253	VSS 346
E14	VSS 254	VSS 347
AV13	VSS 255	VSS 348
AR13	VSS 256	VSS 349
AN13	VSS 257	VSS 350
AM13	VSS 258	VSS 351
AL13	VSS 259	VSS 352
AG13	VSS 260	VSS 353
P13	VSS 261	VSS 354
F13	VSS 262	VSS 355
D13	VSS 263	VSS 356
B13	VSS 264	VSS 357
AY12	VSS 265	VSS 358
AC12	VSS 266	VSS 359
K12	VSS 267	VSS 360
H12	VSS 268	
E12	VSS 269	
AD11	VSS 270	
AA11	VSS 271	
Y11	VSS 272	

VSS

U37D		
DDR A D0	AJ35	SA_DQ0
DDR A D1	AJ34	SA_DQ1
DDR A D2	AM31	SA_DQ2
DDR A D3	AM33	SA_DQ3
DDR A D4	AJ36	SA_DQ4
DDR A D5	AK35	SA_DQ5
DDR A D6	AJ32	SA_DQ6
DDR A D7	AH31	SA_DQ7
DDR A D8	AN35	SA_DQ8
DDR A D9	AP33	SA_DQ9
DDR A D10	AR31	SA_DQ10
DDR A D11	AP31	SA_DQ11
DDR A D12	AN38	SA_DQ12
DDR A D13	AM36	SA_DQ13
DDR A D14	AM34	SA_DQ14
DDR A D15	AN33	SA_DQ15
DDR A D16	AK26	SA_DQ16
DDR A D17	AL27	SA_DQ17
DDR A D18	AM26	SA_DQ18
DDR A D19	AN24	SA_DQ19
DDR A D20	AK28	SA_DQ20
DDR A D21	AL28	SA_DQ21
DDR A D22	AM24	SA_DQ22
DDR A D23	AP26	SA_DQ23
DDR A D24	AR23	SA_DQ24
DDR A D25	AL22	SA_DQ25
DDR A D26	AP21	SA_DQ26
DDR A D27	AN20	SA_DQ27
DDR A D28	AL23	SA_DQ28
DDR A D29	AP24	SA_DQ29
DDR A D30	AR20	SA_DQ30
DDR A D31	AT21	SA_DQ31
DDR A D32	AR12	SA_DQ32
DDR A D33	AR14	SA_DQ33
DDR A D34	AP13	SA_DQ34
DDR A D35	AP12	SA_DQ35
DDR A D36	AT13	SA_DQ36
DDR A D37	AT12	SA_DQ37
DDR A D38	AL14	SA_DQ38
DDR A D39	AL12	SA_DQ39
DDR A D40	AK9	SA_DQ40
DDR A D41	AN7	SA_DQ41
DDR A D42	AK8	SA_DQ42
DDR A D43	AK7	SA_DQ43
DDR A D44	AP9	SA_DQ44
DDR A D45	AN9	SA_DQ45
DDR A D46	AT5	SA_DQ46
DDR A D47	AL5	SA_DQ47
DDR A D48	AY2	SA_DQ48
DDR A D49	AW2	SA_DQ49
DDR A D50	AF1	SA_DQ50
DDR A D51	AN2	SA_DQ51
DDR A D52	AV2	SA_DQ52
DDR A D53	AT3	SA_DQ53
DDR A D54	AN1	SA_DQ54
DDR A D55	AL2	SA_DQ55
DDR A D56	AG7	SA_DQ56
DDR A D57	AF9	SA_DQ57
DDR A D58	AG4	SA_DQ58
DDR A D59	AF6	SA_DQ59
DDR A D60	AG9	SA_DQ60
DDR A D61	AH6	SA_DQ61
DDR A D62	AF4	SA_DQ62
DDR A D63	AF8	SA_DQ63

DDR SYSTEM MEMORY A

DDR A D[0..63] <<>> DDR_A_D[0..63] 12
 DDR A BS[0..2] <<>> DDR_A_BS[0..2] 12,13
 DDR A DM[0..7] <<>> DDR_A_DM[0..7] 12
 DDR A DQS[0..7] <<>> DDR_A_DQS[0..7] 12
 DDR A DQS#[0..7] <<>> DDR_A_DQS#[0..7] 12
 DDR A MA[0..13] <<>> DDR_A_MA[0..13] 12,13

SA_BS_0 AY12 DDR A BS0
 SA_BS_1 AV14 DDR A BS1
 SA_BS_2 BA20 DDR A BS2
 SA_CAS# AY13 DDR A CAS#>>>DDR_A_CAS# 12,13
 SA_DM_0 AJ33 DDR A DM0
 SA_DM_1 AM35 DDR A DM1
 SA_DM_2 AL26 DDR A DM2
 SA_DM_3 AN22 DDR A DM3
 SA_DM_4 AM14 DDR A DM4
 SA_DM_5 AL9 DDR A DM5
 SA_DM_6 AR3 DDR A DM6
 SA_DM_7 AH4 DDR A DM7
 SA_DQS_0 AK33 DDR A DQS0
 SA_DQS_1 AT33 DDR A DQS1
 SA_DQS_2 AN28 DDR A DQS2
 SA_DQS_3 AM22 DDR A DQS3
 SA_DQS_4 AN12 DDR A DQS4
 SA_DQS_5 AN8 DDR A DQS5
 SA_DQS_6 AP3 DDR A DQS6
 SA_DQS_7 AG5 DDR A DQS7
 SA_DQS#_0 AK32 DDR A DQS#0
 SA_DQS#_1 AU33 DDR A DQS#1
 SA_DQS#_2 AM27 DDR A DQS#2
 SA_DQS#_3 AM21 DDR A DQS#3
 SA_DQS#_4 AM12 DDR A DQS#4
 SA_DQS#_5 AL8 DDR A DQS#5
 SA_DQS#_6 AN3 DDR A DQS#6
 SA_DQS#_7 AH5 DDR A DQS#7
 SA_MA_0 AY16 DDR A MA0
 SA_MA_1 AU14 DDR A MA1
 SA_MA_2 AW16 DDR A MA2
 SA_MA_3 BA16 DDR A MA3
 SA_MA_4 BA17 DDR A MA4
 SA_MA_5 AU16 DDR A MA5
 SA_MA_6 AU17 DDR A MA6
 SA_MA_7 AU17 DDR A MA7
 SA_MA_8 AW17 DDR A MA8
 SA_MA_9 AT16 DDR A MA9
 SA_MA_10 AU13 DDR A MA10
 SA_MA_11 AT17 DDR A MA11
 SA_MA_12 AV20 DDR A MA12
 SA_MA_13 AV12 DDR A MA13
 SA_RAS# AW14 DDR A RAS#>>>DDR_A_RAS# 12,13
 SA_RCVENIN# AK23 M A RCVENIN# TP3 RAS# TPAD28
 SA_RCVENOUT# AK24 M A RCVENOUT# TP2 TPAD28
 SA_WE# AY14 DDR A WE#>>>DDR_A_WE# 12,13

U37E		
DDR B D0	AK39	SB_DQ0
DDR B D1	AJ37	SB_DQ1
DDR B D2	AP39	SB_DQ2
DDR B D3	AR41	SB_DQ3
DDR B D4	AJ38	SB_DQ4
DDR B D5	AK38	SB_DQ5
DDR B D6	AN41	SB_DQ6
DDR B D7	AP41	SB_DQ7
DDR B D8	AT40	SB_DQ8
DDR B D9	AV41	SB_DQ9
DDR B D10	AU38	SB_DQ10
DDR B D11	AV38	SB_DQ11
DDR B D12	AP38	SB_DQ12
DDR B D13	AR40	SB_DQ13
DDR B D14	AW38	SB_DQ14
DDR B D15	AY38	SB_DQ15
DDR B D16	BA38	SB_DQ16
DDR B D17	AV36	SB_DQ17
DDR B D18	AR36	SB_DQ18
DDR B D19	AP36	SB_DQ19
DDR B D20	BA36	SB_DQ20
DDR B D21	AU36	SB_DQ21
DDR B D22	AP34	SB_DQ22
DDR B D23	AV34	SB_DQ23
DDR B D24	AY34	SB_DQ24
DDR B D25	BA33	SB_DQ25
DDR B D26	AT31	SB_DQ26
DDR B D27	AU29	SB_DQ27
DDR B D28	AU31	SB_DQ28
DDR B D29	AW31	SB_DQ29
DDR B D30	AV29	SB_DQ30
DDR B D31	AW29	SB_DQ31
DDR B D32	AM19	SB_DQ32
DDR B D33	AL19	SB_DQ33
DDR B D34	AP14	SB_DQ34
DDR B D35	AN14	SB_DQ35
DDR B D36	AN17	SB_DQ36
DDR B D37	AM16	SB_DQ37
DDR B D38	AP15	SB_DQ38
DDR B D39	AL15	SB_DQ39
DDR B D40	AJ11	SB_DQ40
DDR B D41	AH10	SB_DQ41
DDR B D42	AJ9	SB_DQ42
DDR B D43	AK10	SB_DQ43
DDR B D44	AK13	SB_DQ44
DDR B D45	AH11	SB_DQ45
DDR B D46	AK10	SB_DQ46
DDR B D47	AJ8	SB_DQ47
DDR B D48	BA10	SB_DQ48
DDR B D49	AW10	SB_DQ49
DDR B D50	BA4	SB_DQ50
DDR B D51	AW4	SB_DQ51
DDR B D52	AY10	SB_DQ52
DDR B D53	AY9	SB_DQ53
DDR B D54	AW5	SB_DQ54
DDR B D55	AY5	SB_DQ55
DDR B D56	AV4	SB_DQ56
DDR B D57	AK4	SB_DQ57
DDR B D58	AK3	SB_DQ58
DDR B D59	AK3	SB_DQ59
DDR B D60	AT4	SB_DQ60
DDR B D61	AK5	SB_DQ61
DDR B D62	AJ5	SB_DQ62
DDR B D63	AJ3	SB_DQ63

DDR SYSTEM MEMORY B

DDR B D[0..63] <<>> DDR_B_D[0..63] 13
 DDR B BS[0..2] <<>> DDR_B_BS[0..2] 12,13
 DDR B DM[0..7] <<>> DDR_B_DM[0..7] 13
 DDR B DQS[0..7] <<>> DDR_B_DQS[0..7] 13
 DDR B DQS#[0..7] <<>> DDR_B_DQS#[0..7] 13
 DDR B MA[0..13] <<>> DDR_B_MA[0..13] 12,13

SB_BS_0 AT24 DDR B BS0
 SB_BS_1 AV23 DDR B BS1
 SB_BS_2 AY28 DDR B BS2
 SB_CAS# AR24 DDR B CAS#>>>DDR_B_CAS# 12,13
 SB_DM_0 AK36 DDR B DM0
 SB_DM_1 AR38 DDR B DM1
 SB_DM_2 AT36 DDR B DM2
 SB_DM_3 BA31 DDR B DM3
 SB_DM_4 AL17 DDR B DM4
 SB_DM_5 AH8 DDR B DM5
 SB_DM_6 BA5 DDR B DM6
 SB_DM_7 AN4 DDR B DM7
 SB_DQS_0 AM39 DDR B DQS0
 SB_DQS_1 AT39 DDR B DQS1
 SB_DQS_2 AU35 DDR B DQS2
 SB_DQS_3 AR29 DDR B DQS3
 SB_DQS_4 AR16 DDR B DQS4
 SB_DQS_5 AR10 DDR B DQS5
 SB_DQS_6 AR7 DDR B DQS6
 SB_DQS_7 AN5 DDR B DQS7
 SB_DQS#_0 AM40 DDR B DQS#0
 SB_DQS#_1 AU39 DDR B DQS#1
 SB_DQS#_2 AT35 DDR B DQS#2
 SB_DQS#_3 AP29 DDR B DQS#3
 SB_DQS#_4 AP16 DDR B DQS#4
 SB_DQS#_5 AT10 DDR B DQS#5
 SB_DQS#_6 AT7 DDR B DQS#6
 SB_DQS#_7 AP5 DDR B DQS#7
 SB_MA_0 AY23 DDR B MA0
 SB_MA_1 AW24 DDR B MA1
 SB_MA_2 AY24 DDR B MA2
 SB_MA_3 AR28 DDR B MA3
 SB_MA_4 AT27 DDR B MA4
 SB_MA_5 AT28 DDR B MA5
 SB_MA_6 AU27 DDR B MA6
 SB_MA_7 AV28 DDR B MA7
 SB_MA_8 AV27 DDR B MA8
 SB_MA_9 AW27 DDR B MA9
 SB_MA_10 AV24 DDR B MA10
 SB_MA_11 BA27 DDR B MA11
 SB_MA_12 AY27 DDR B MA12
 SB_MA_13 AR23 DDR B MA13
 SB_RAS# AU23 DDR B RAS#>>>DDR_B_RAS# 12,13
 SB_RCVENIN# AK16 M B RCVENIN# TP3 RAS# TPAD28
 SB_RCVENOUT# AK18 M B RCVENOUT# TP2 TPAD28
 SB_WE# AR27 DDR B WE#>>>DDR_B_WE# 12,13

D

C

B

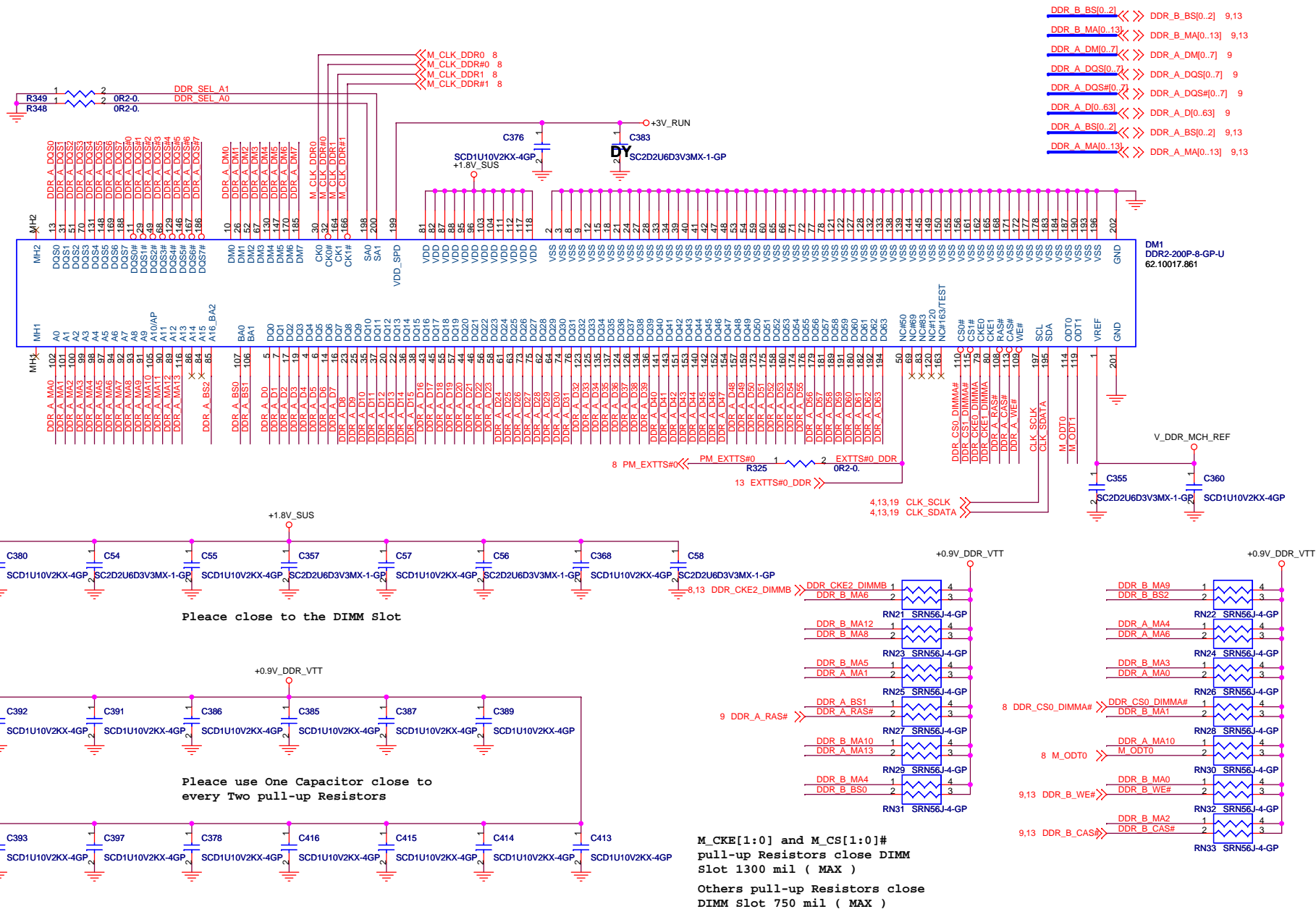
A

D

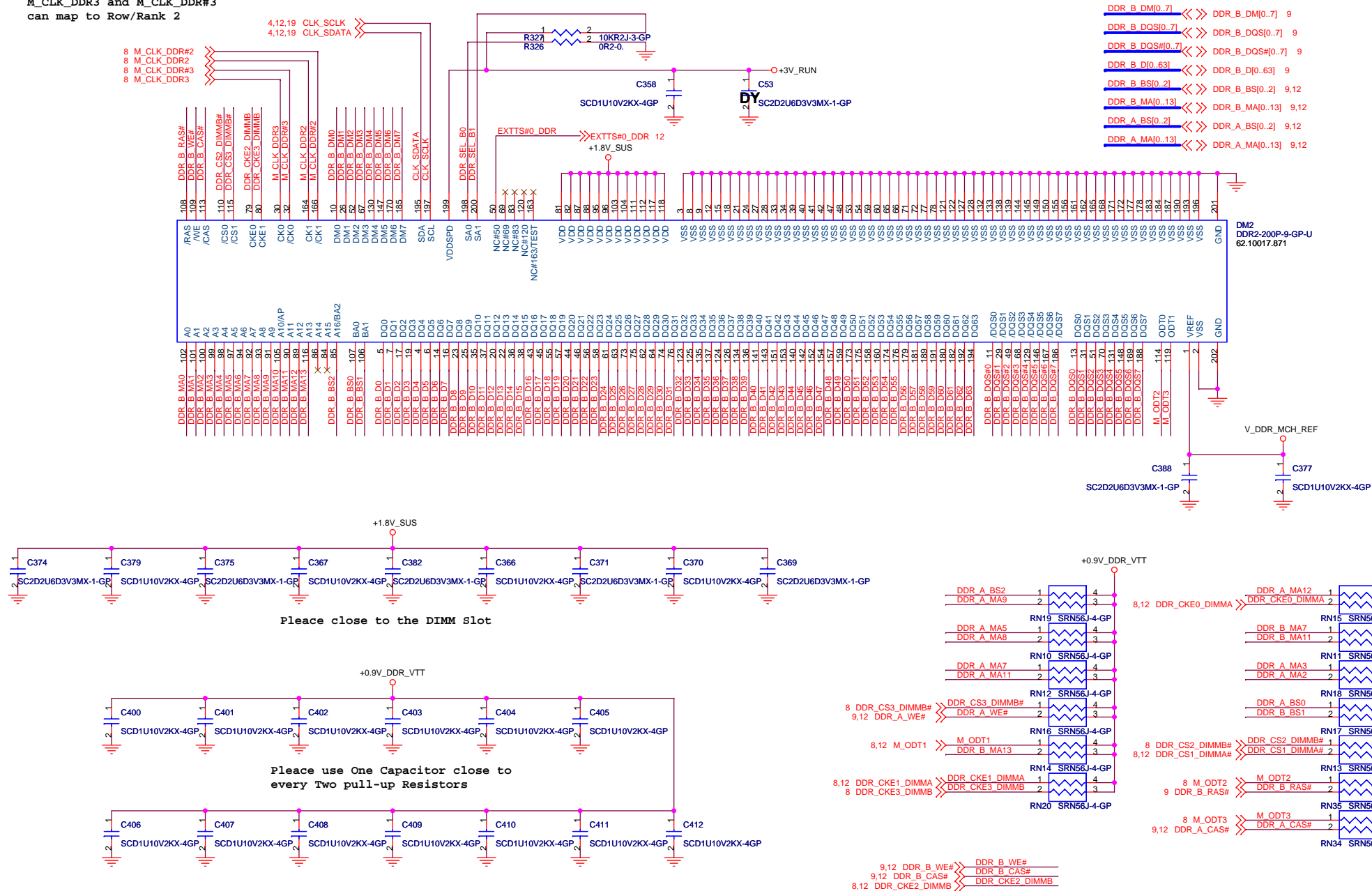
C

B

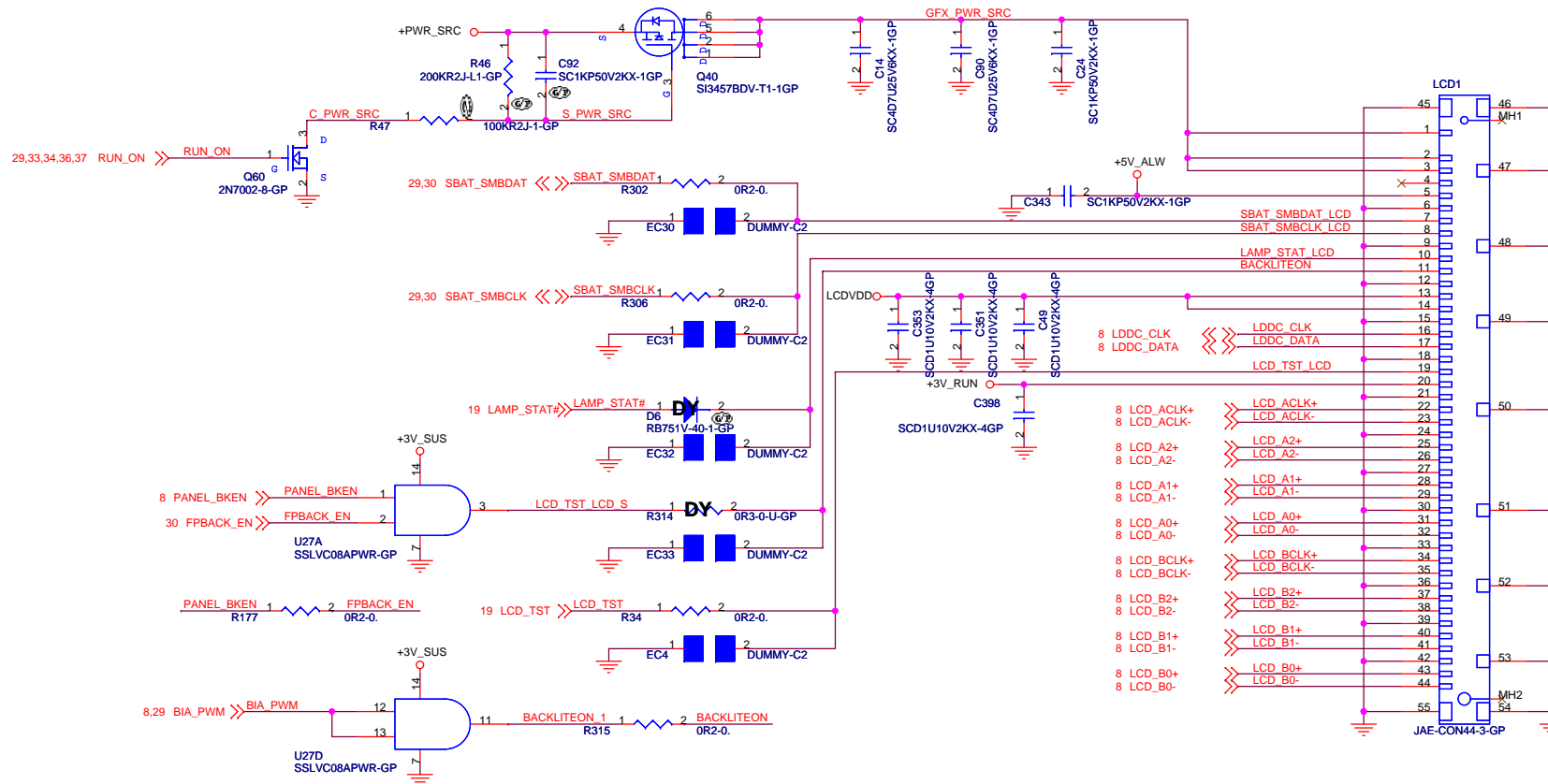
A



M_CLK_DDR3 and M_CLK_DDR#3
can map to Row/Rank 2



SSID = VIDEO



M00 support D05 Inverter

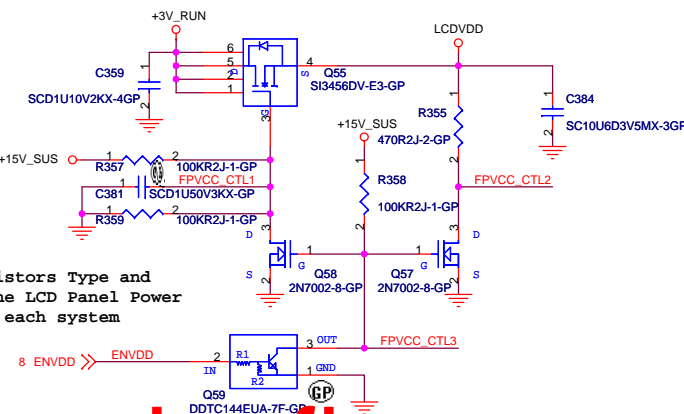
M'07 Inverter support : Populate this Two Resister and

De-populate this SSLVC08APWR

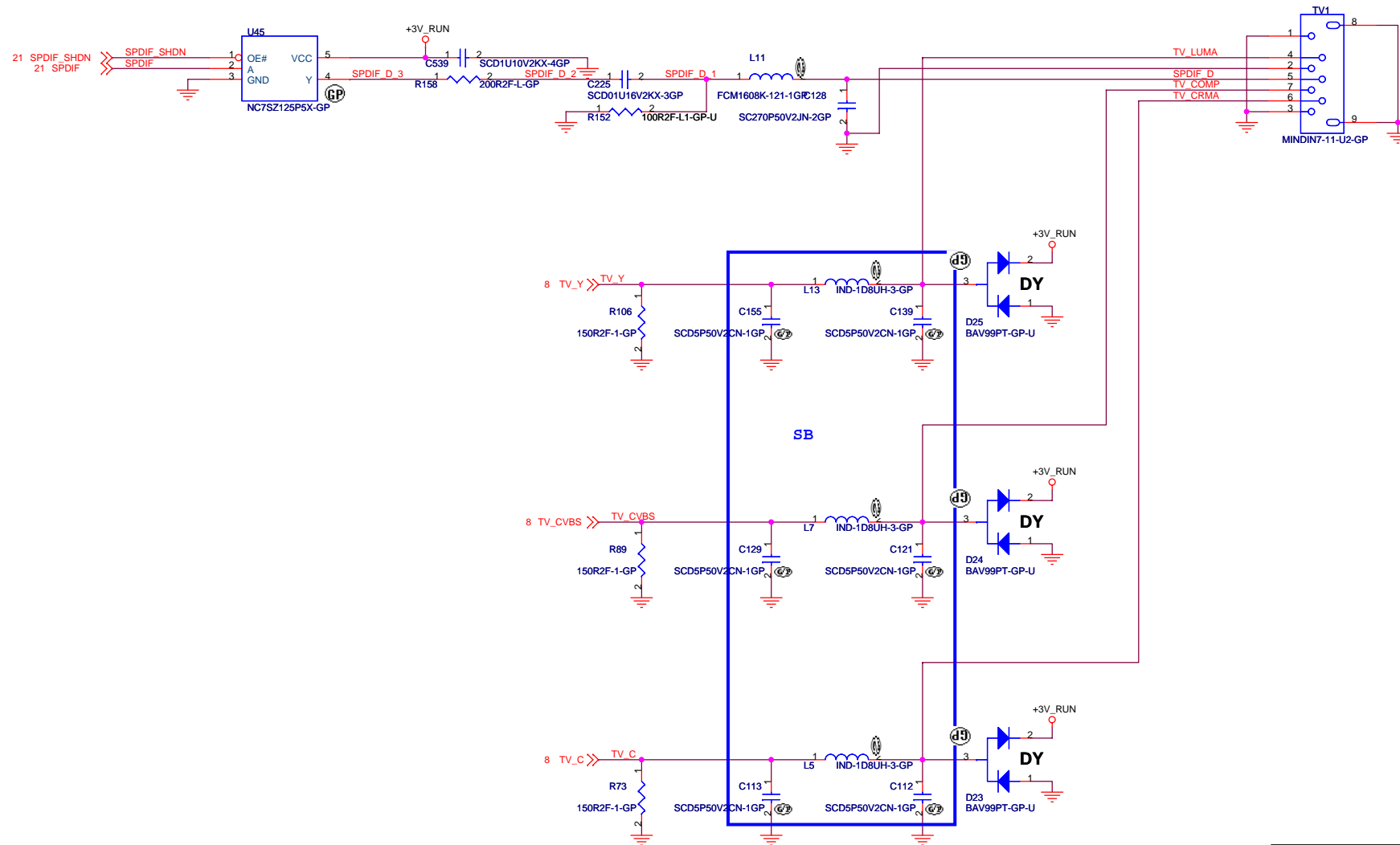
D'05 Inverter support : De-populate this Two Resister and

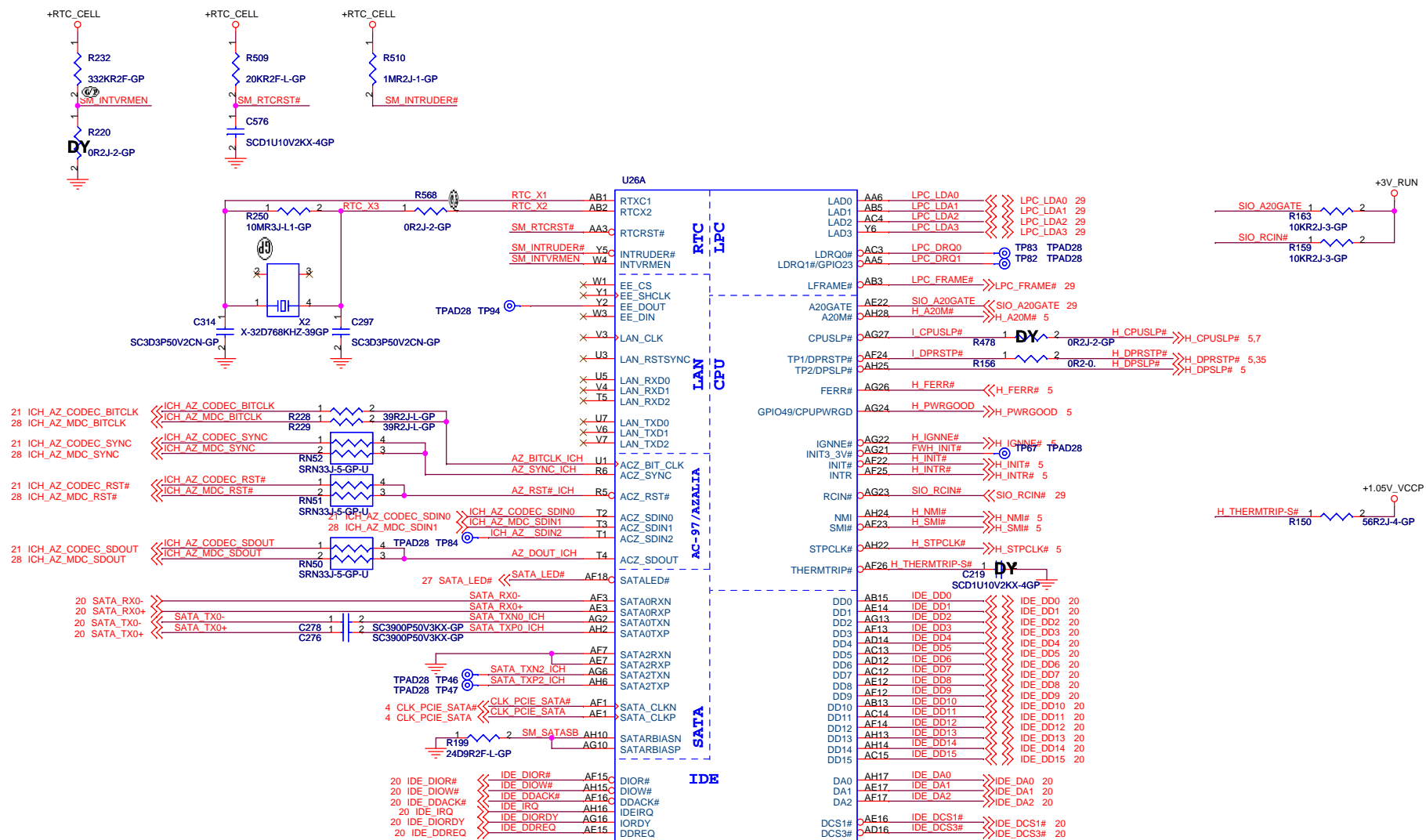
Populate this SSLVC08APWR

Choose the Transistors Type and
Rating base on the LCD Panel Power
requirements for each system

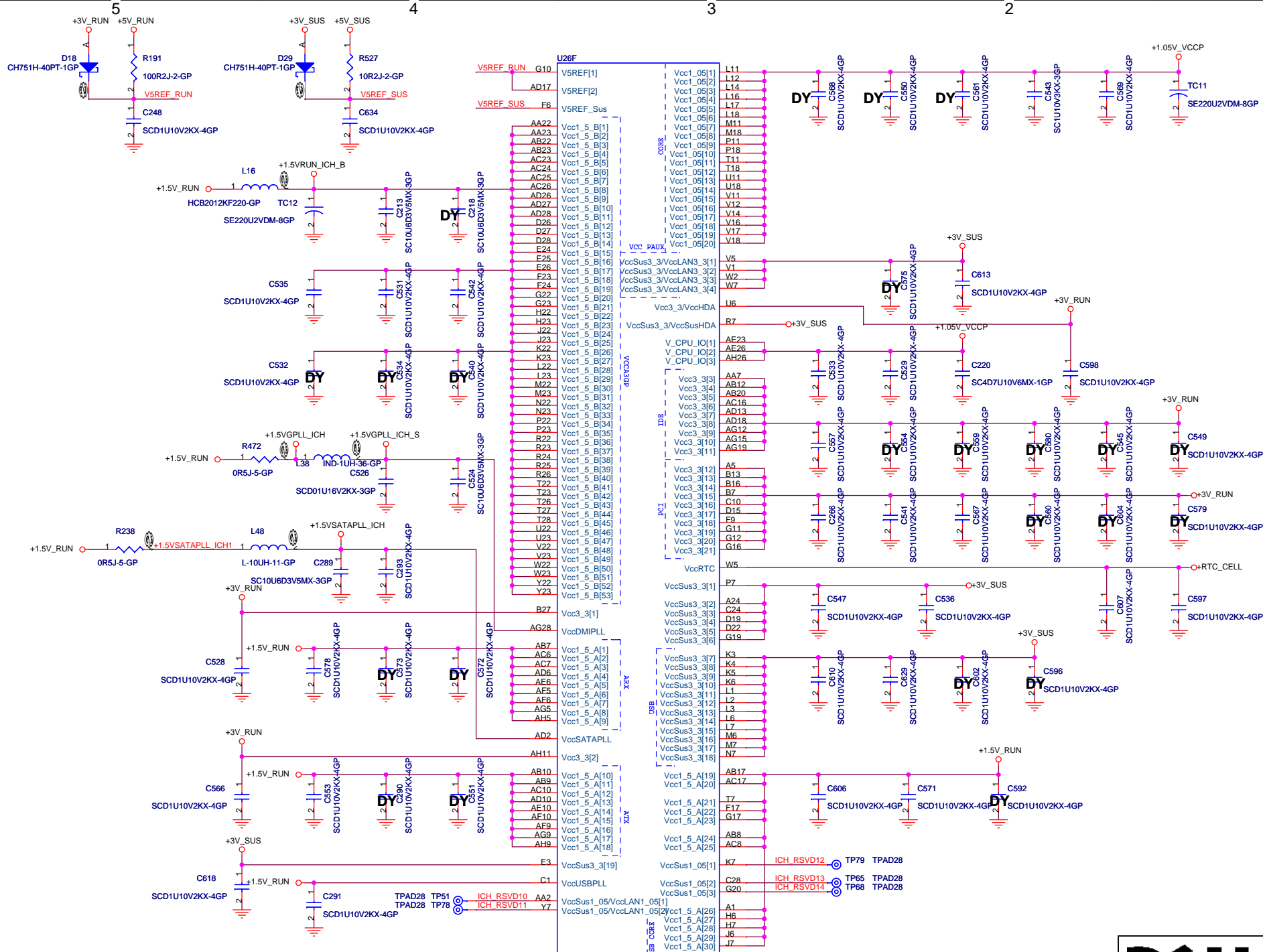


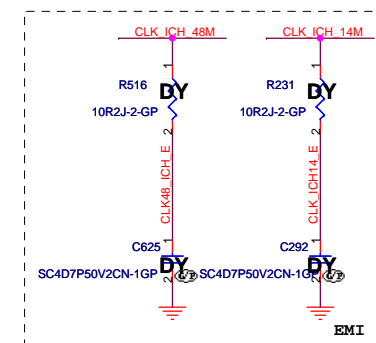
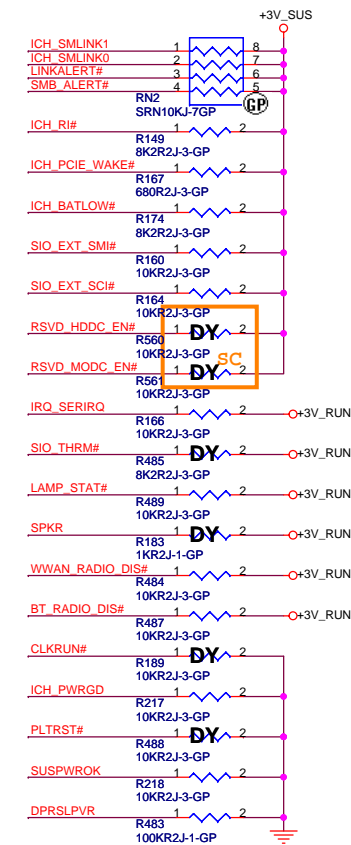
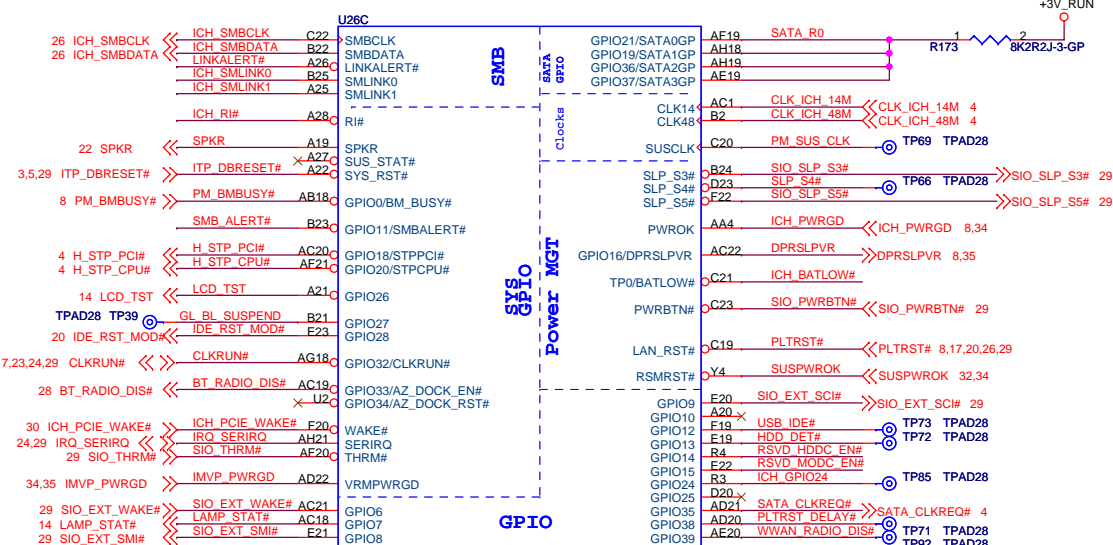
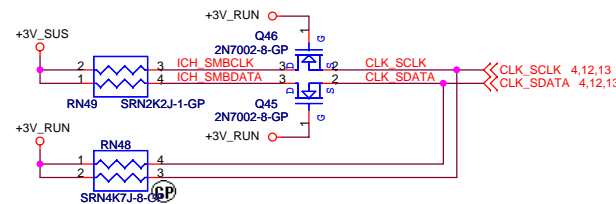
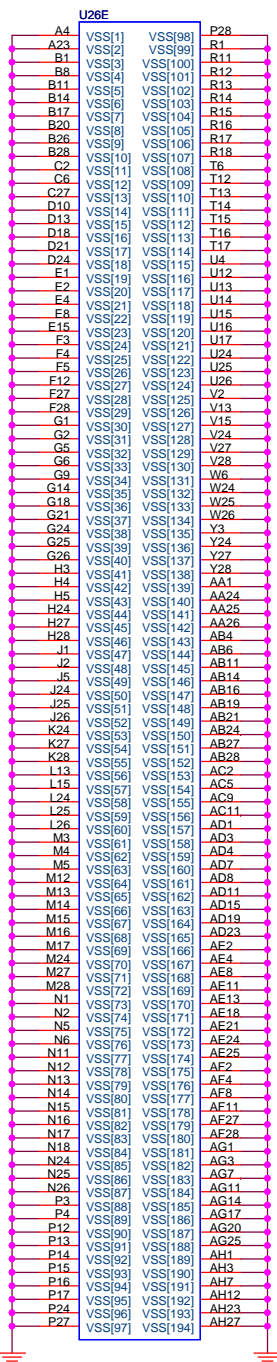
SSID = VIDEO





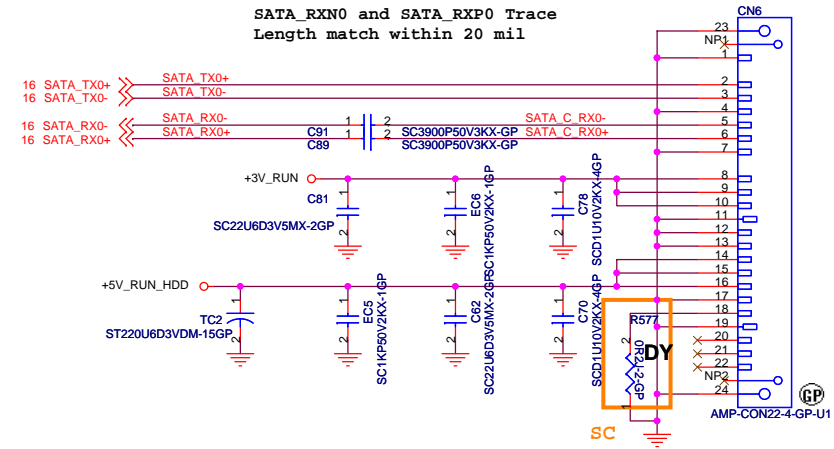
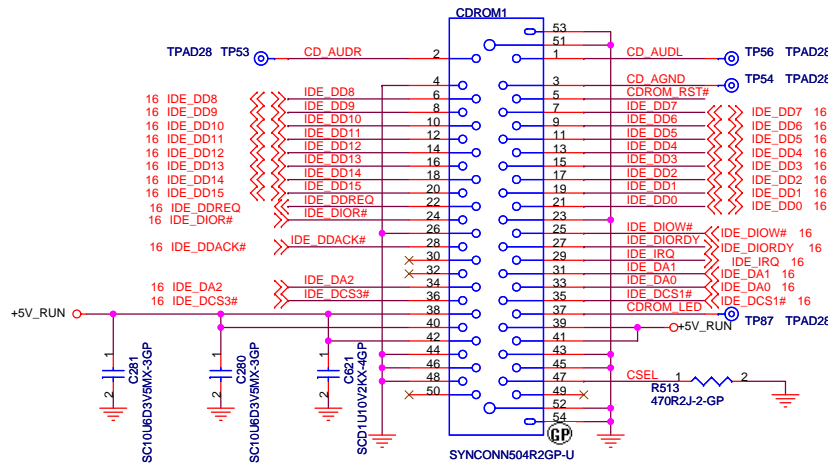
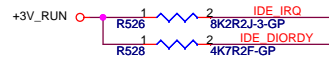
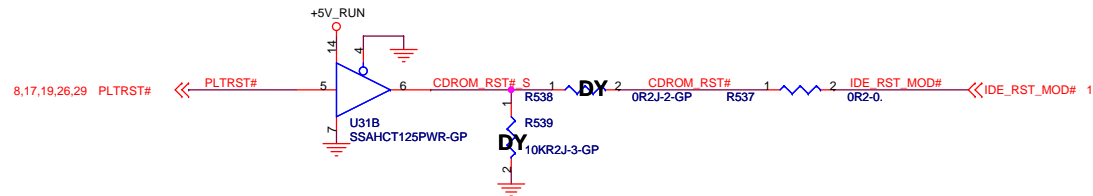
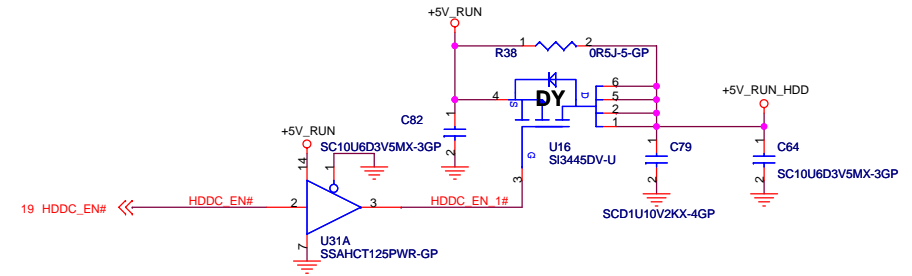






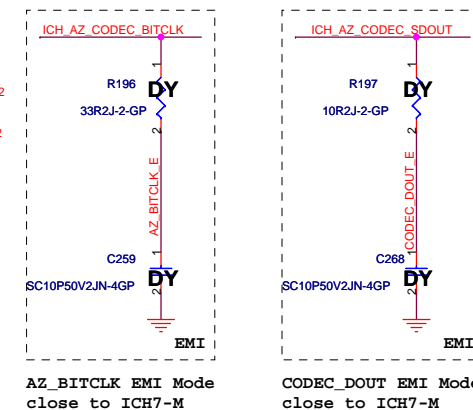
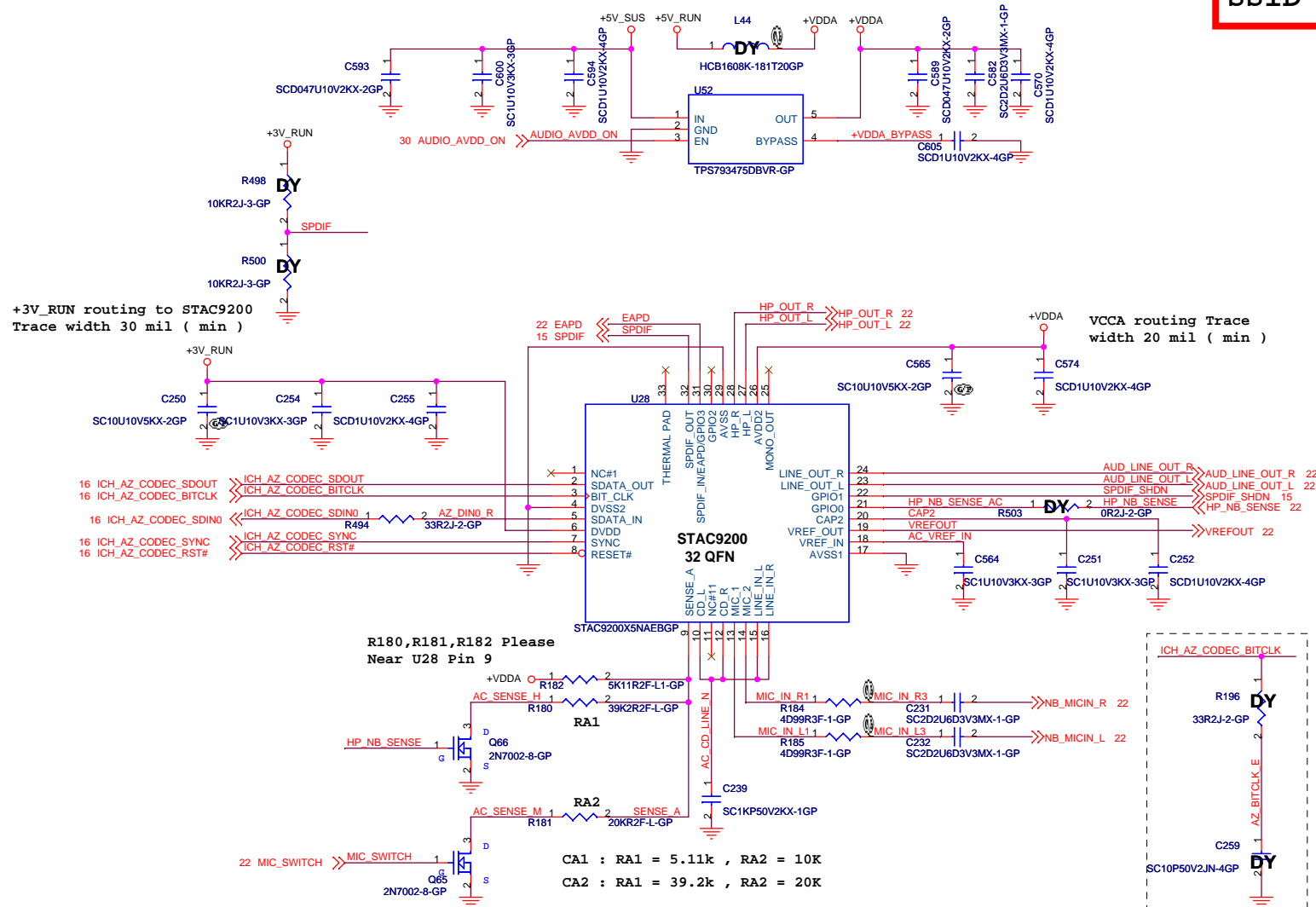
CLK48_ICH and CLK_ICH14 EMI
Mode close to ICH7-M

SSID = IDE & SATA



SATA HD Connector

SSID = AUDIO

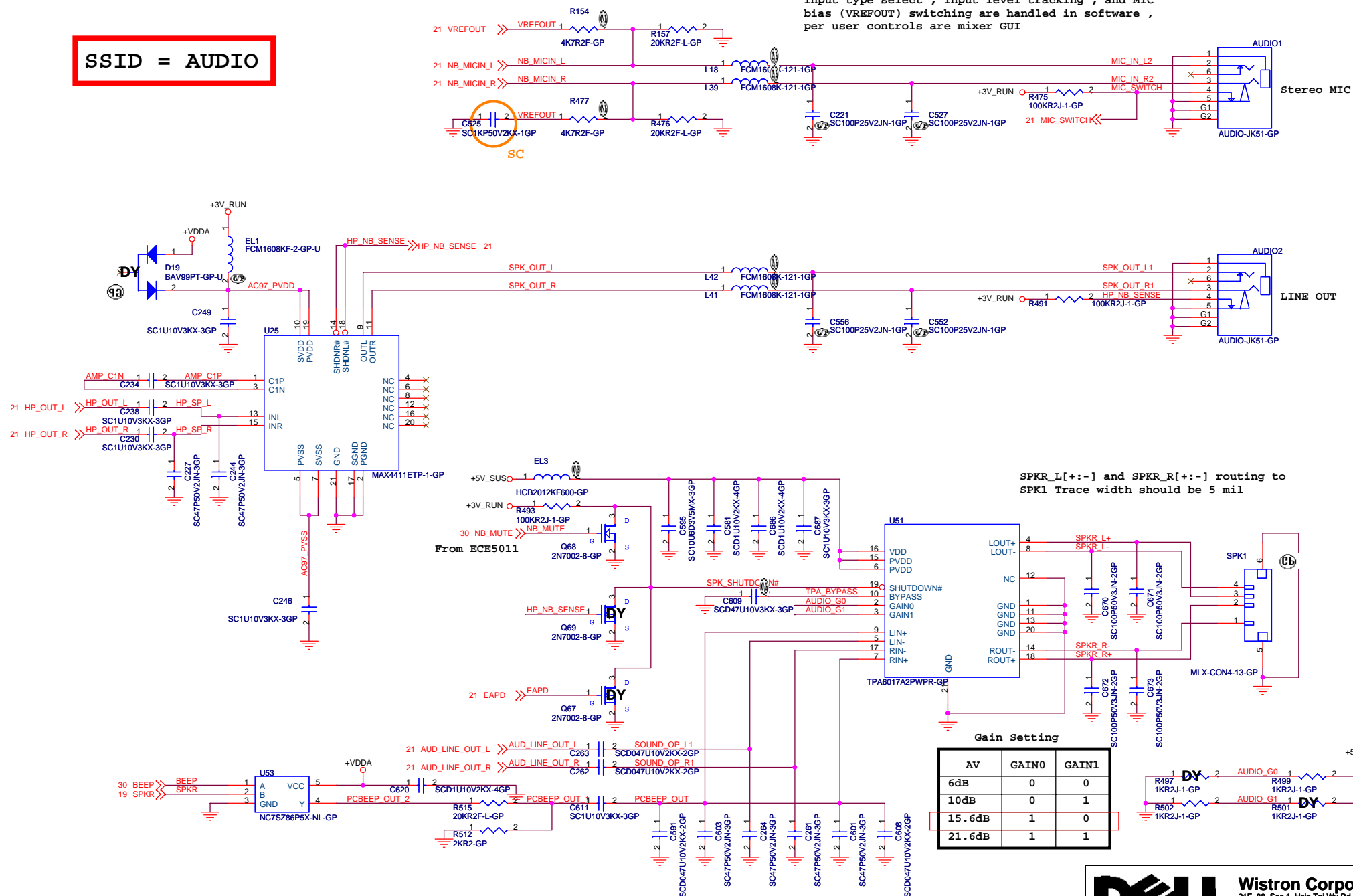


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Title			
AUDIO - 01 - STAC9200			
Size	Document Number	Rev	
A3		-1	
Date:	Wednesday, March 01, 2006	Sheet	21 of 45

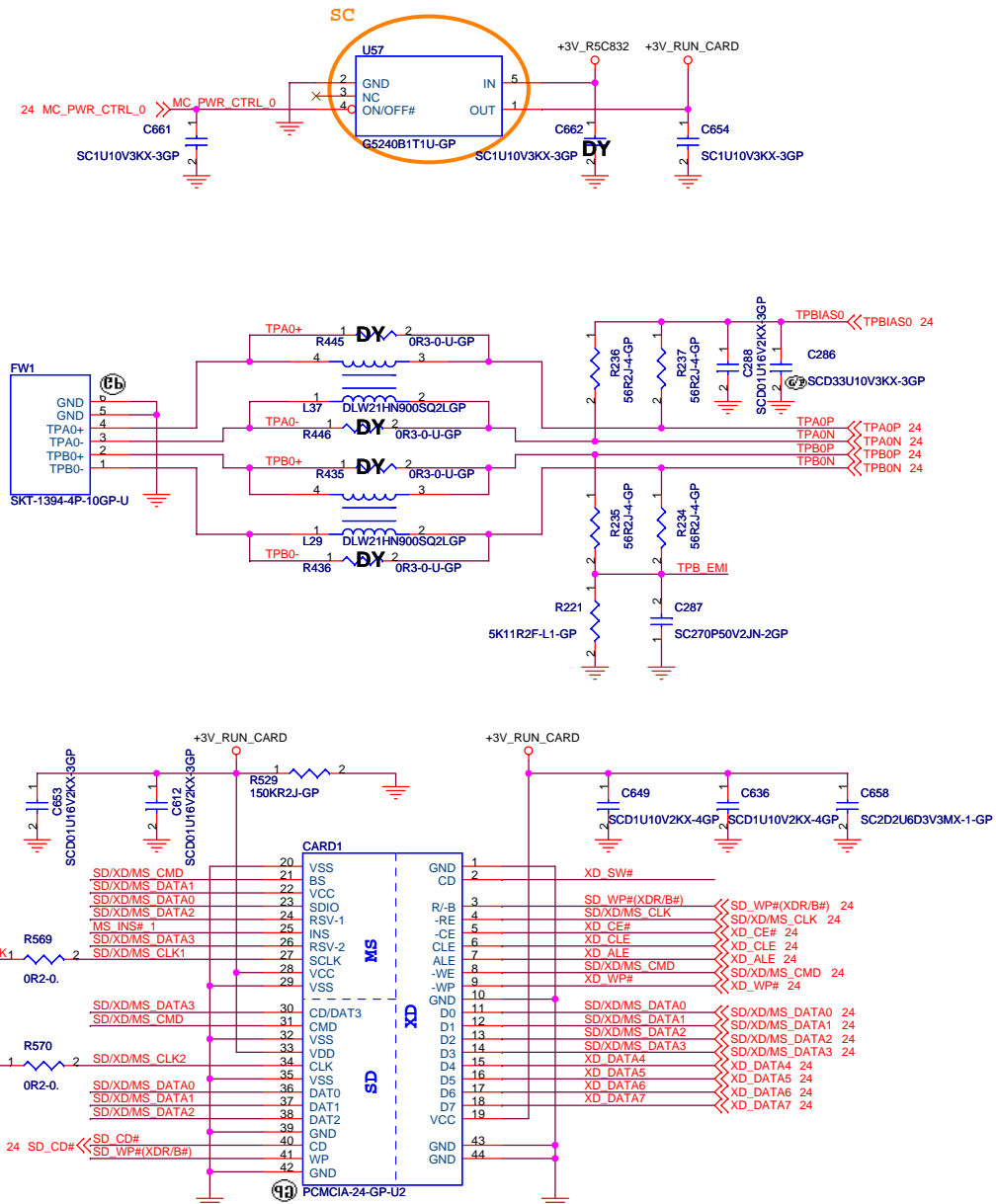
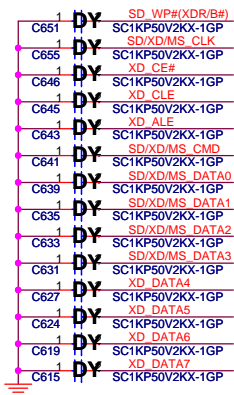
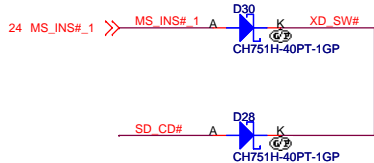
SSID = AUDIO

Input type select , input level tracking , and MIC bias (VREFOUT) switching are handled in software , per user controls are mixer GUI



AV	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1

SSID = 1394



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Title

1394 - 4 IN 1 Connector

Size

Document Number

Bermuda

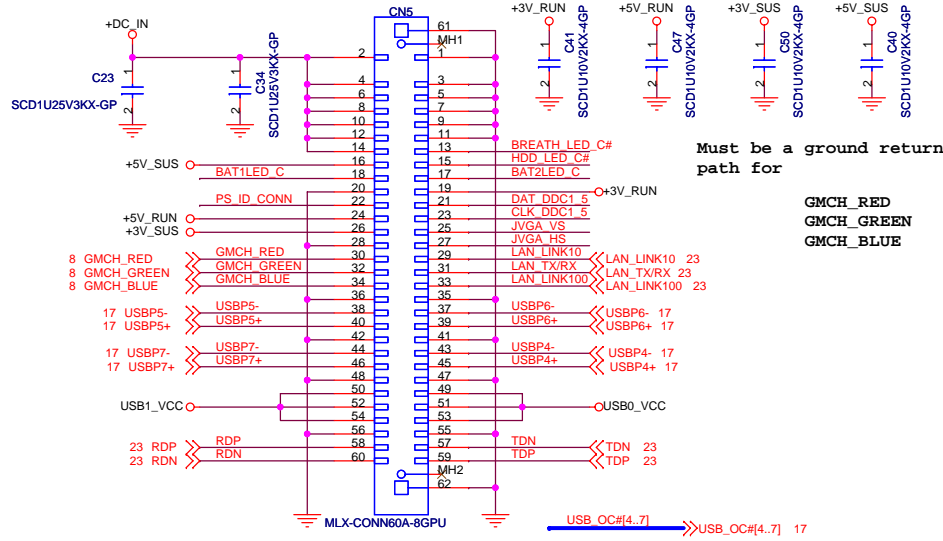
-1

Date: Wednesday, March 01, 2006

Sheet 25 of 45

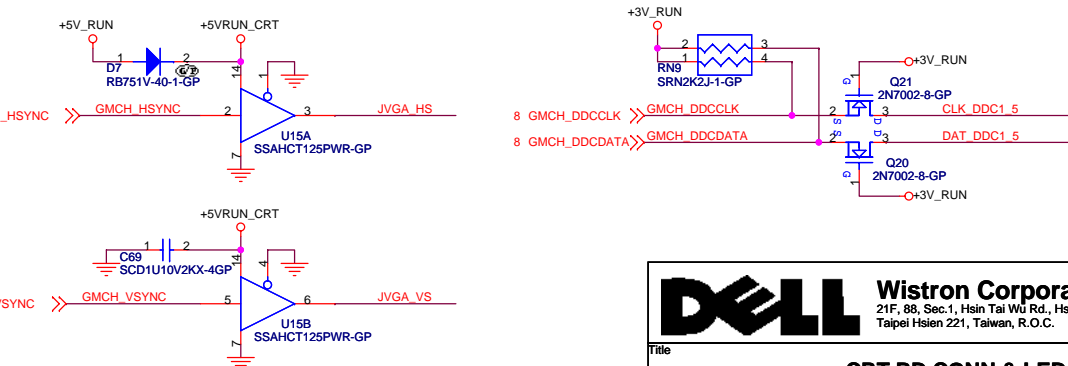
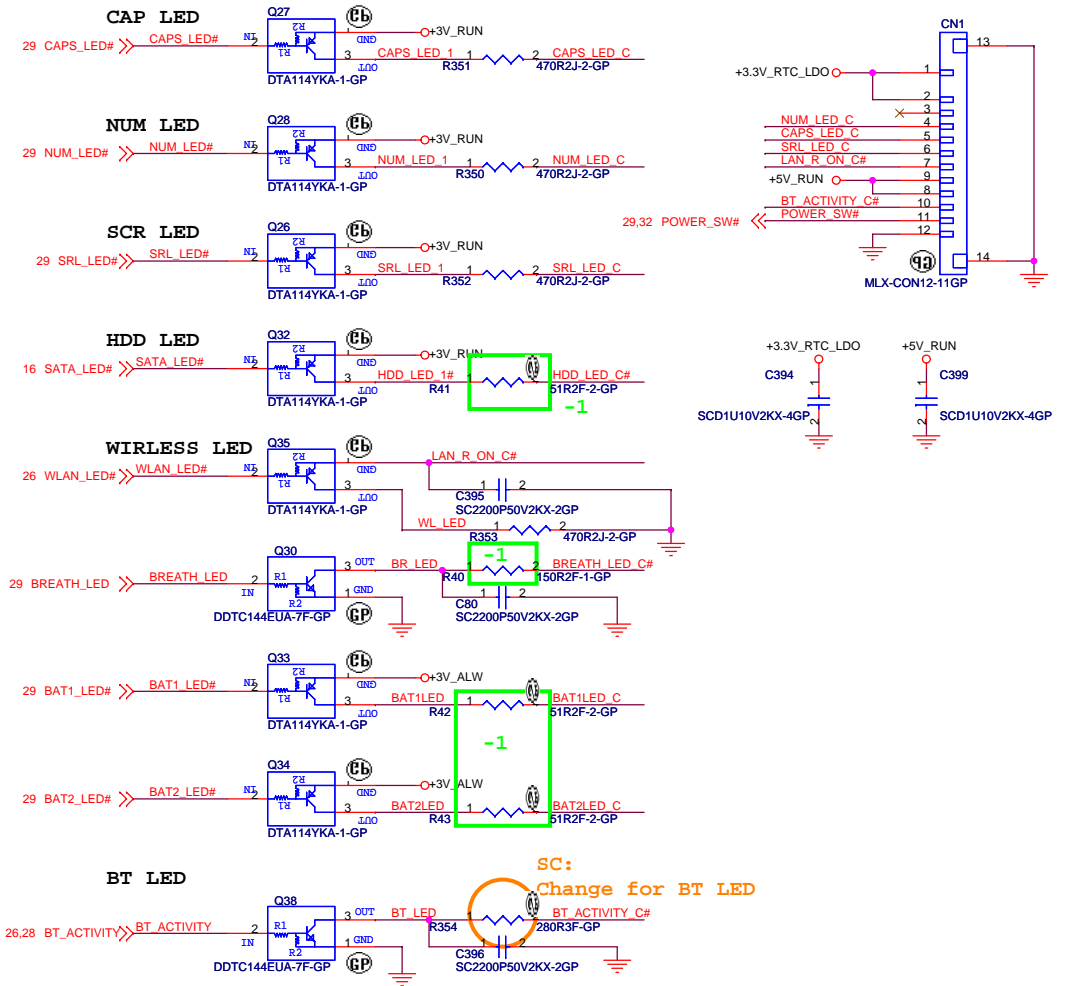
www.vinafix.vn

CRT BD Conn

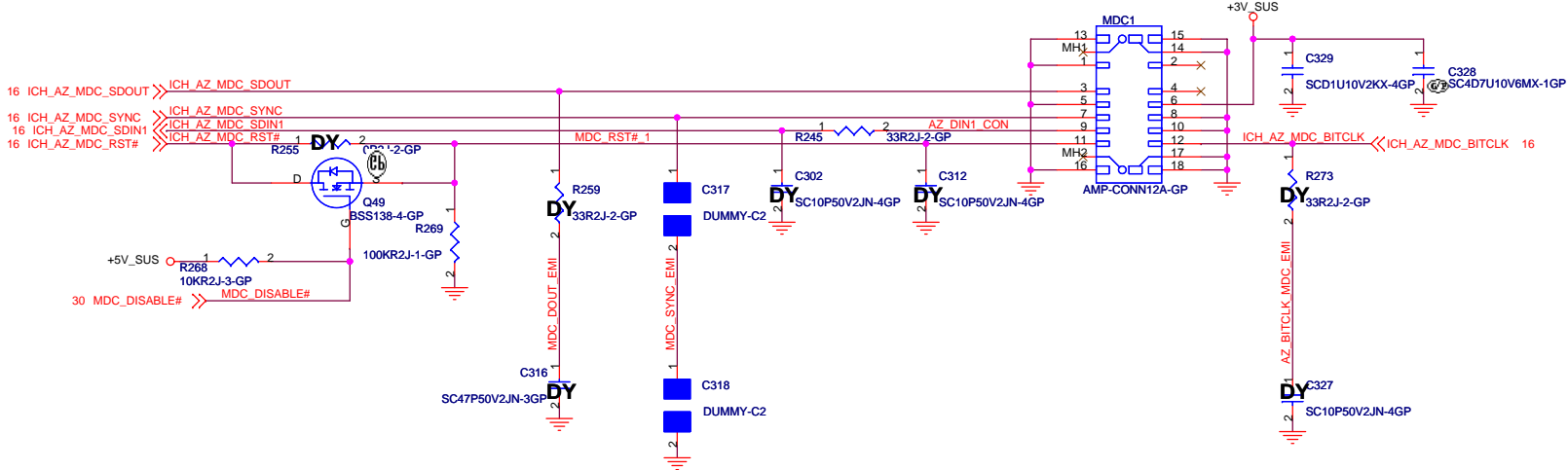


Must be a ground return path for

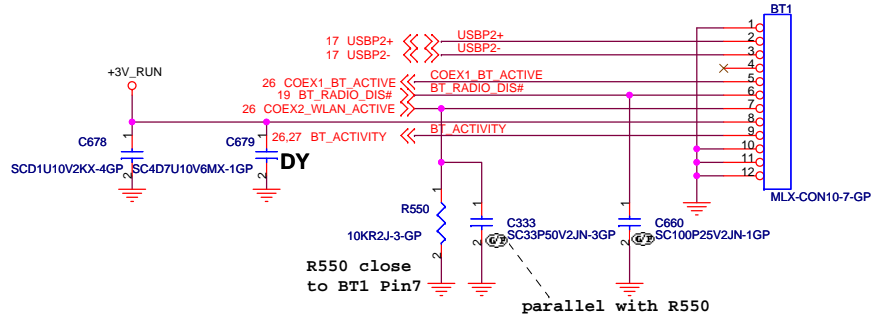
GMCH_RED
GMCH_GREEN
GMCH_BLUE

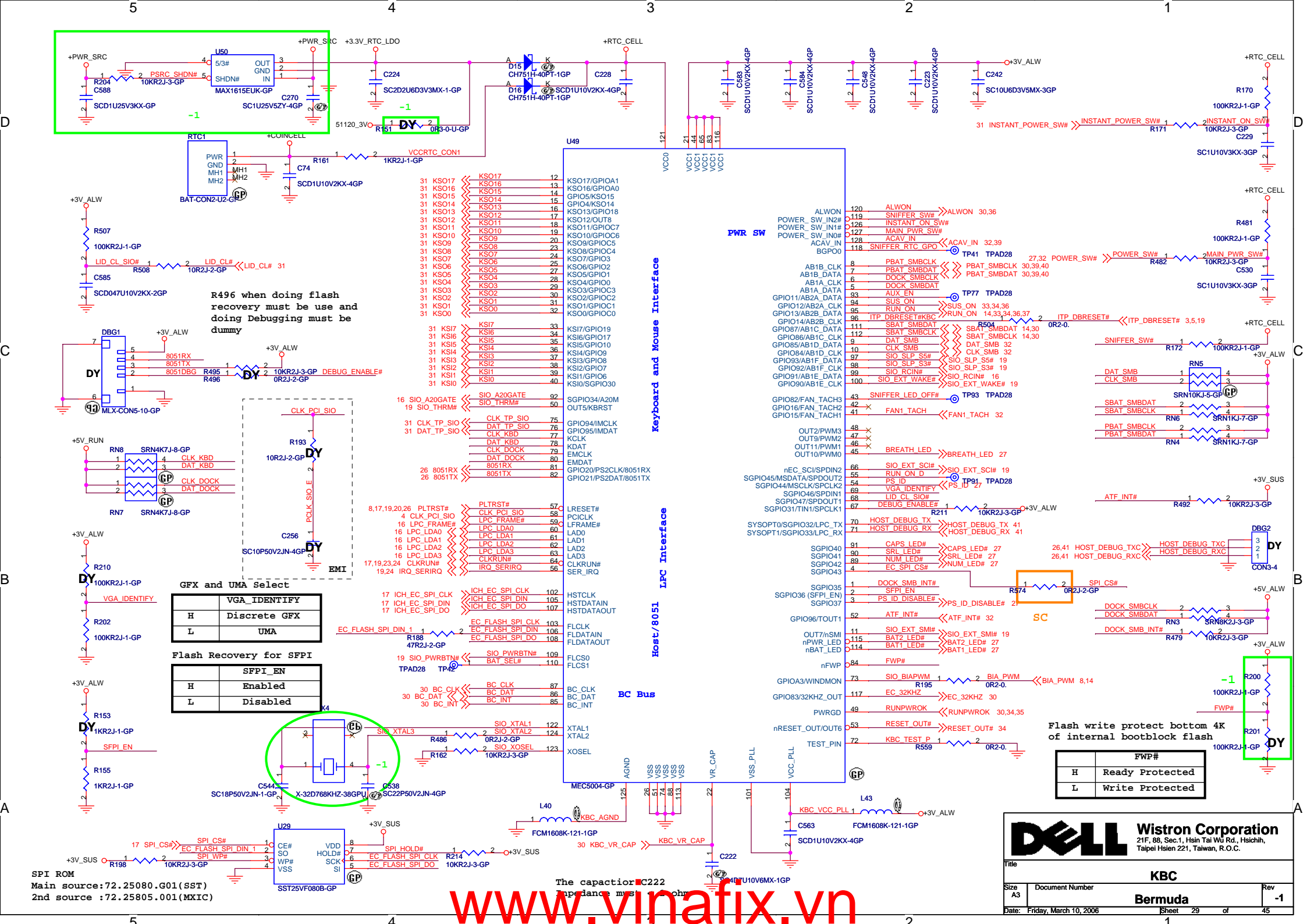


(Not Standard Type)



Bluetooth Module conn.





R496 when doing flash recovery must be use and doing Debugging must be dummy

GFX and UMA Select	
VGA_IDENTIFY	
H	Discrete GFX
L	UMA


Flash Recovery for SFPI	
SFPI_EN	
H	Enabled
L	Disabled

Flash write protect bottom 4K of internal bootblock flash	
FWP#	
H	Ready Protected
L	Write Protected

SPI ROM
Main source : 72.25080.G01 (SST)
2nd source : 72.25805.001 (MXIC)

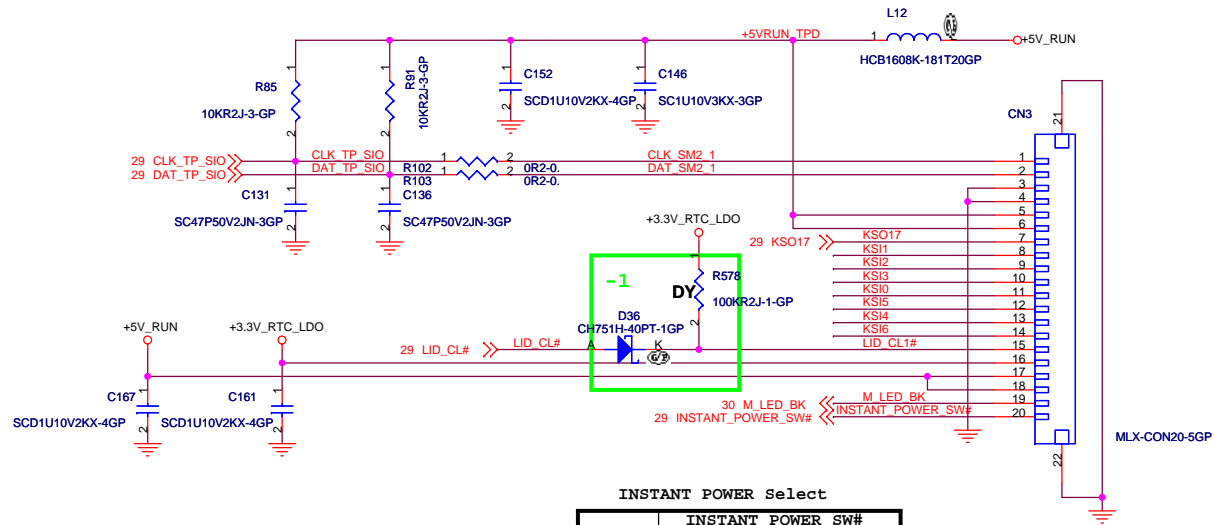
The capacitor C222
Impedance must be 100 ohm

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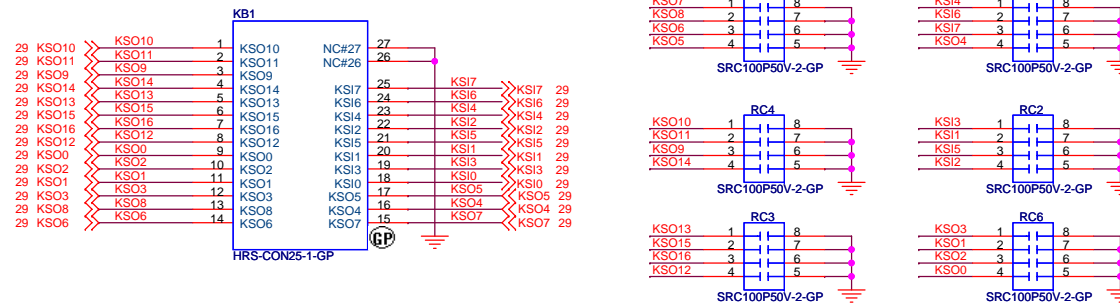


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KBC		
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Media PlayBack / TouchPAD Connector



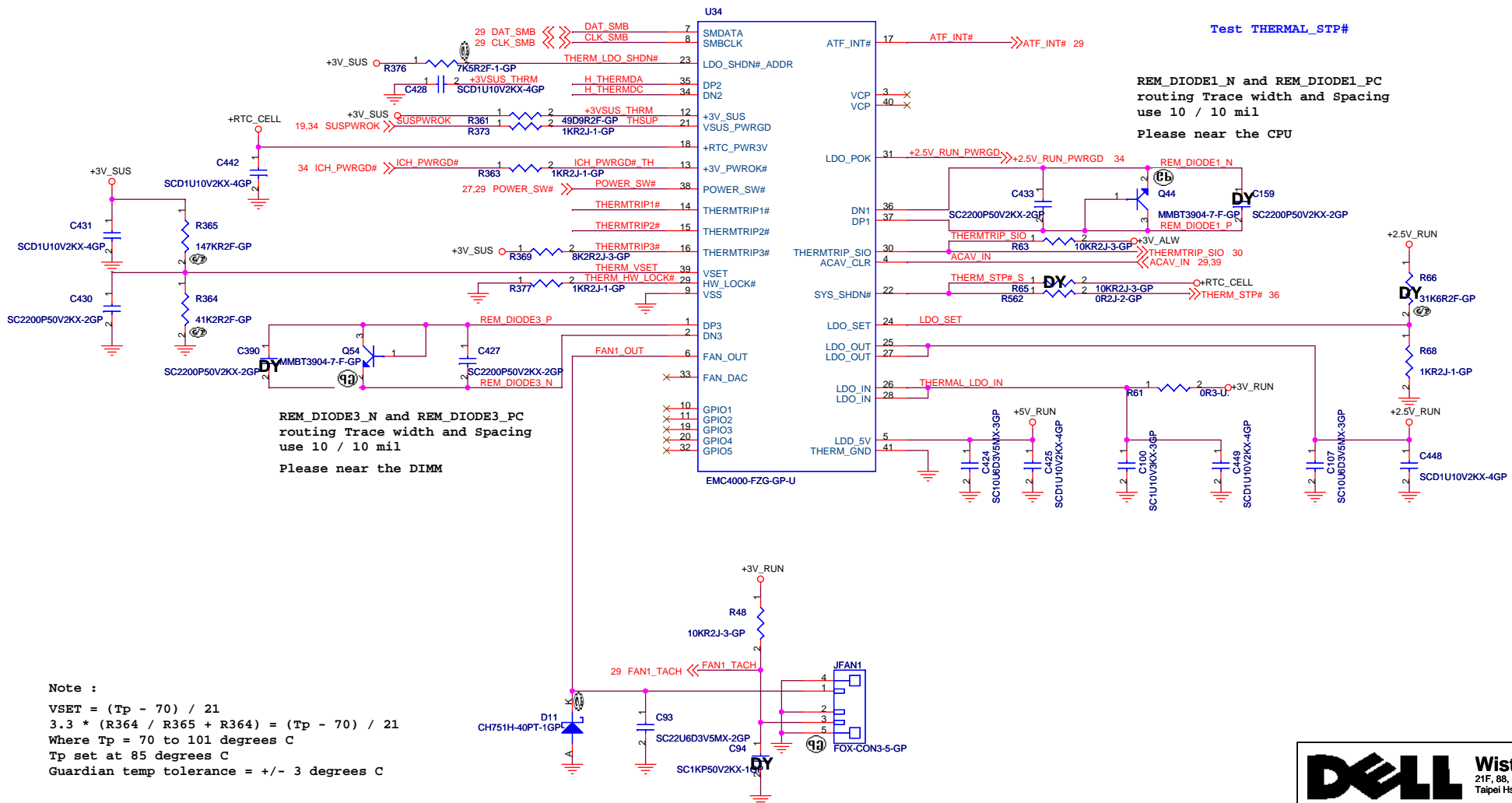
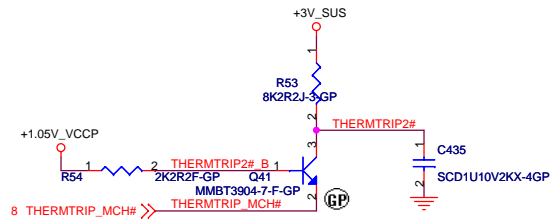
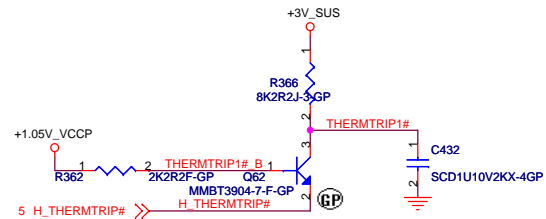
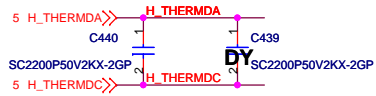
SSID = THERMAL

H_THERMDA and H_THERMDC
routing Trace width and
Spacing use 10 / 10 mil

```

Reserve area near CPU
for a cap between
DP2/DN2

```



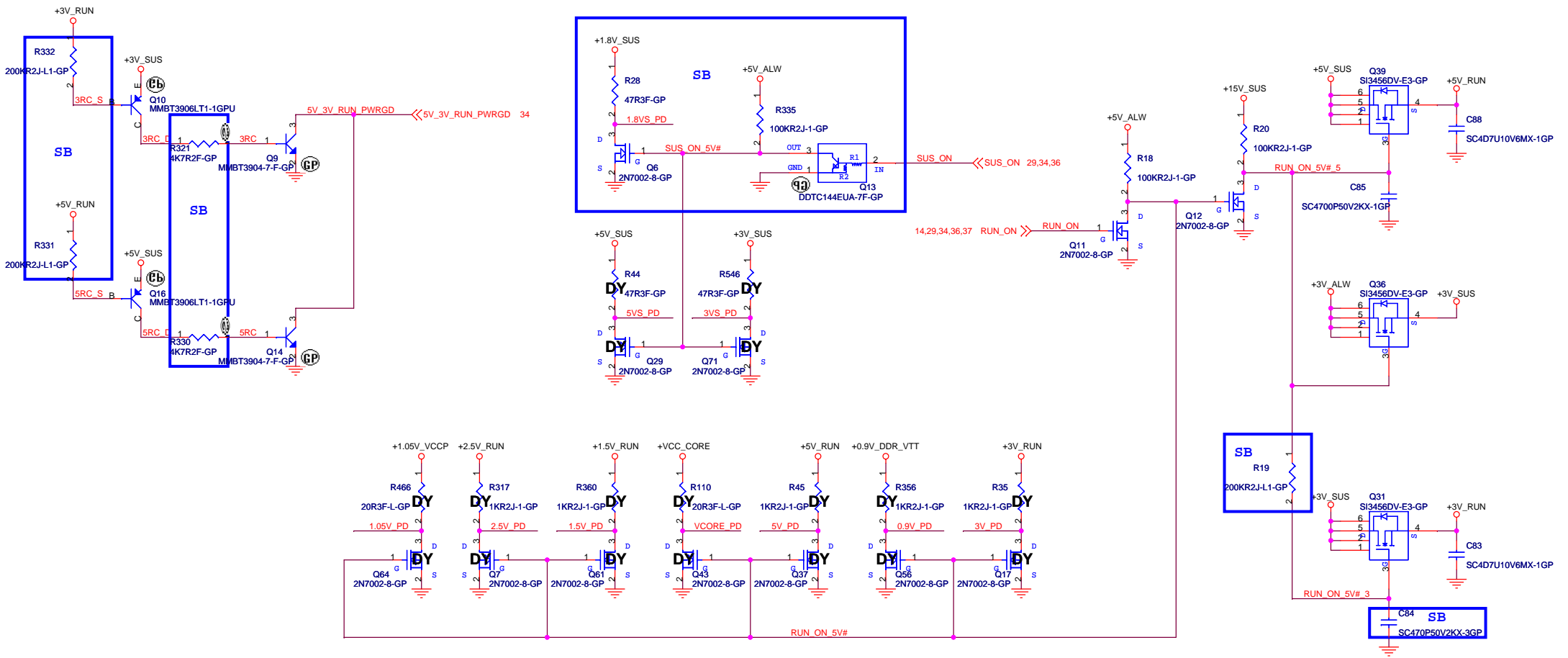
Note :

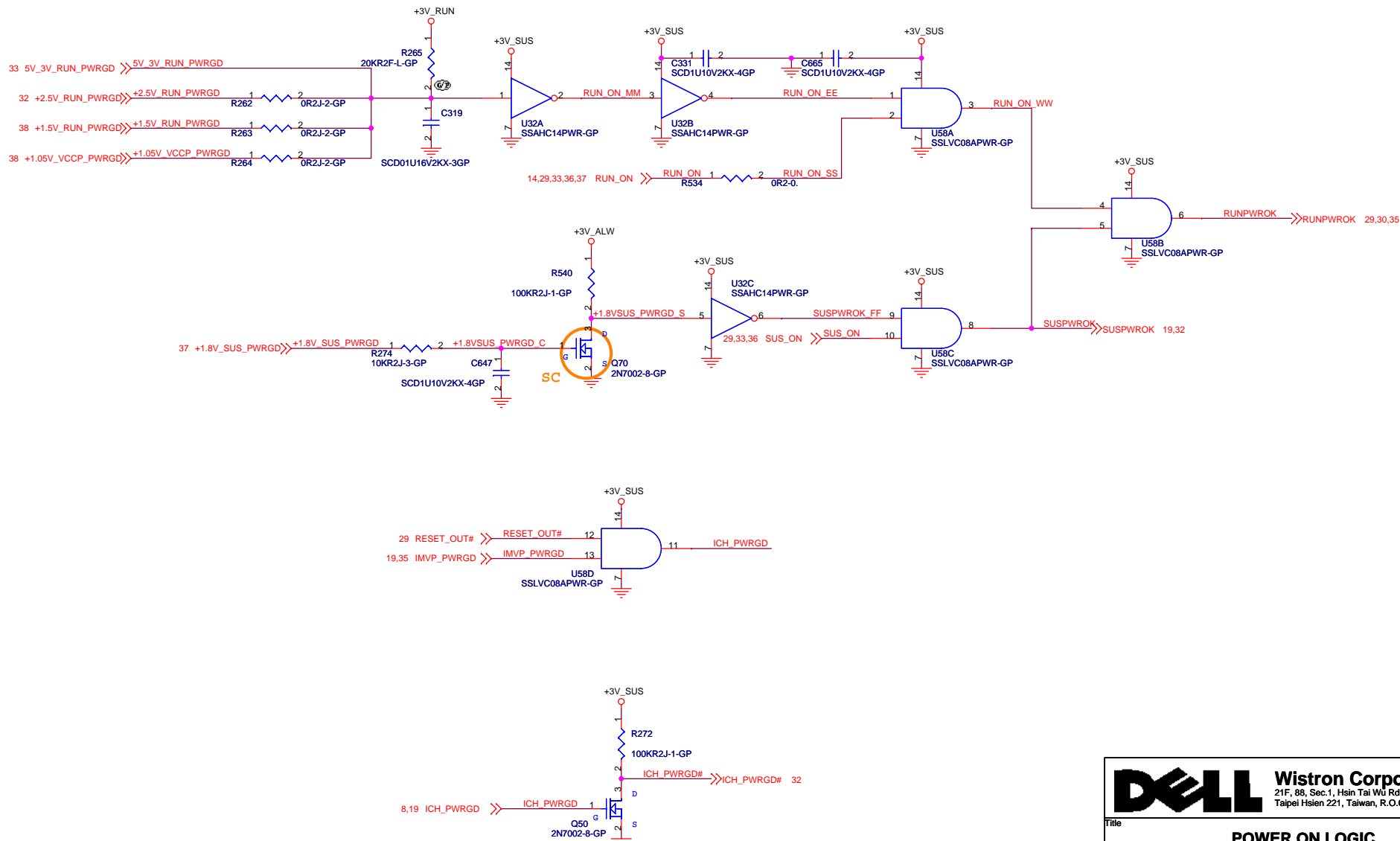
$$VSET = (T_p - 70) / 21$$
$$3.3 * (R_{364} / R_{365} + R_{364}) = (T_p - 70) / 21$$

Where $T_p = 70$ to 101 degrees C

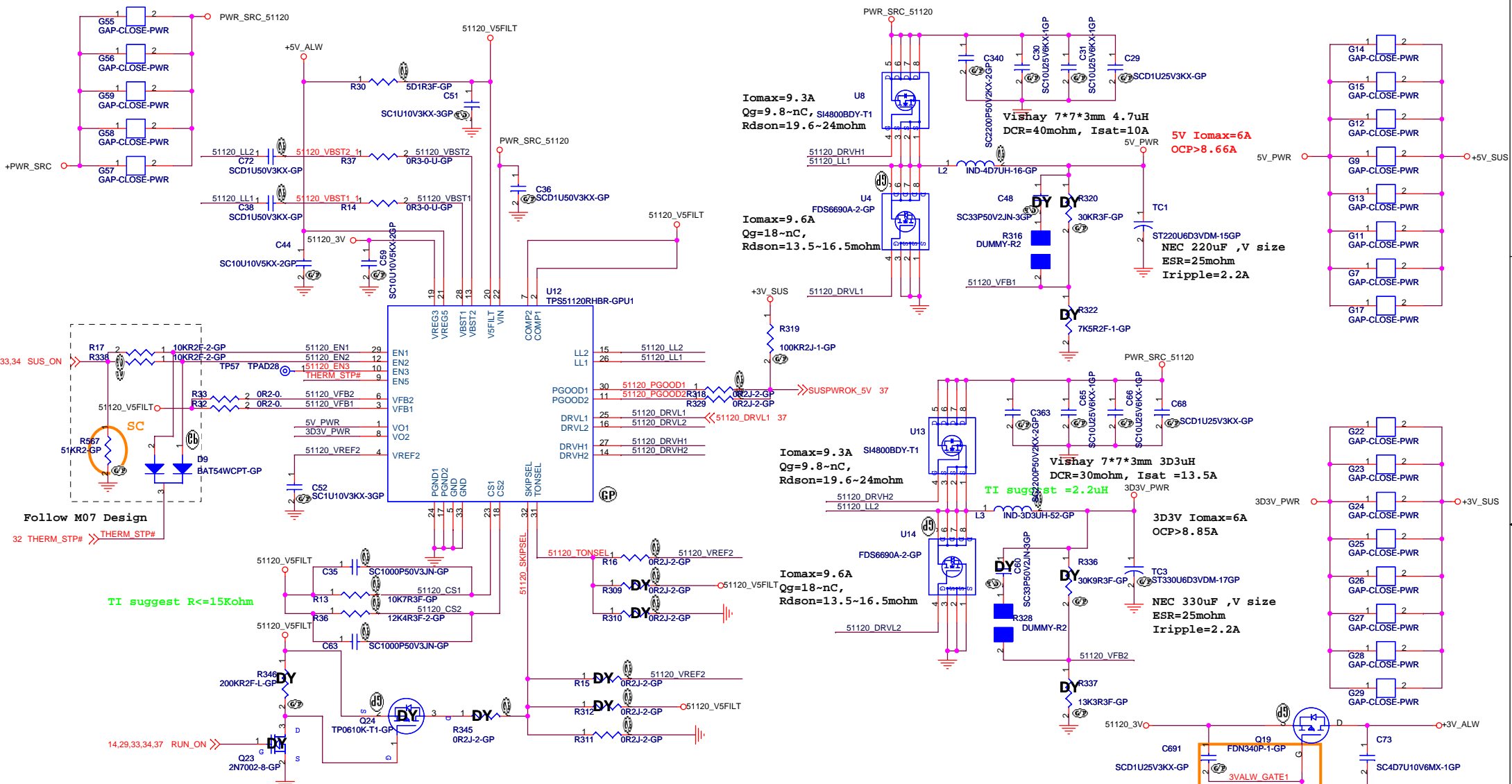
T_p set at 85 degrees C

Guardian temp tolerance = ± 3 degrees C









Follow M07 Design

32 THERM_STP# >> THERM_STP#

TI suggest R<15Kohm

14,29,33,34,37 RUN_ON >>

$$V_{out} = 1V \cdot (R1 + R2) / R2$$

For TPS51120,
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

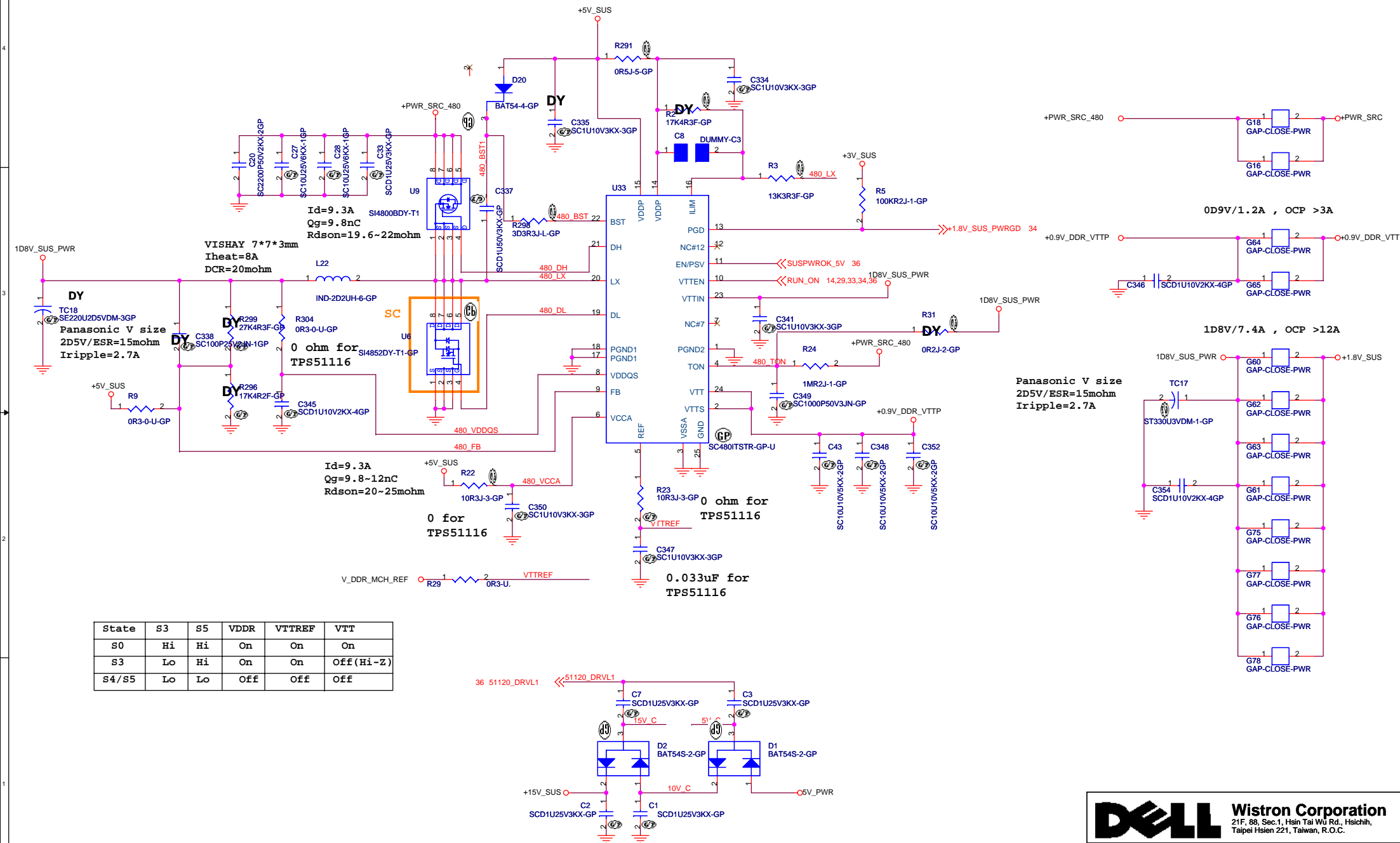
Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

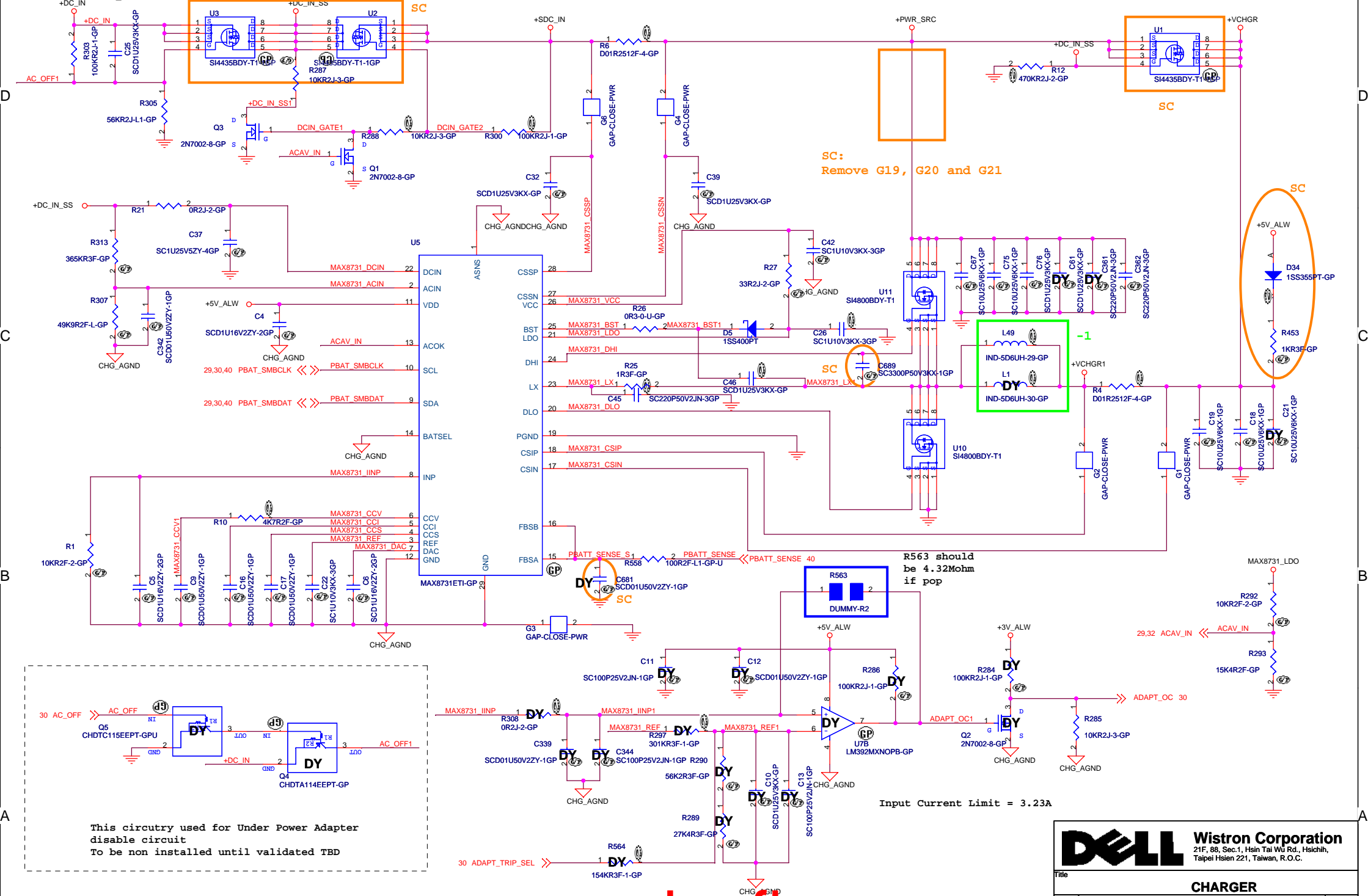
	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on



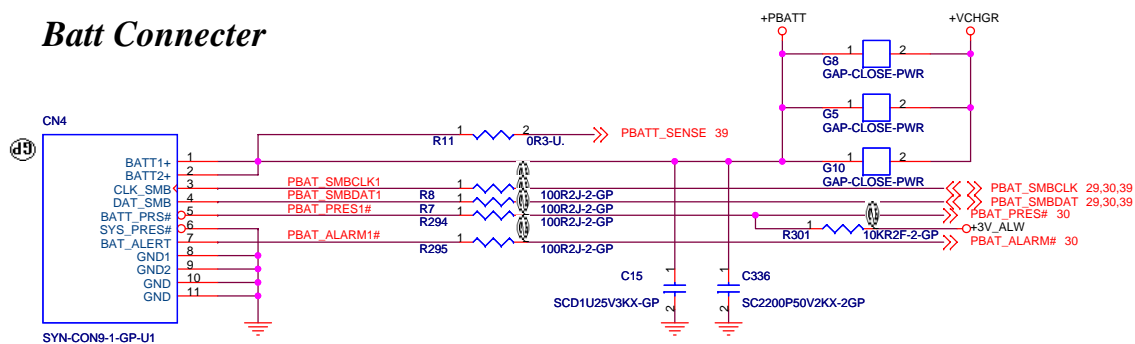
SC480 for 1D8V and 0D9V



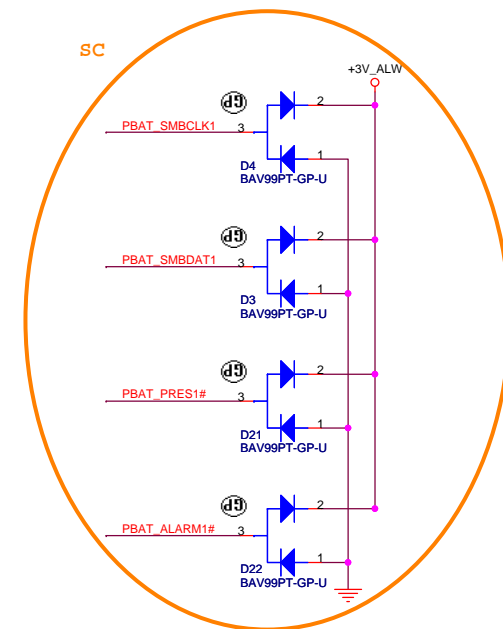
Adaptor In Soft-Start Circuit

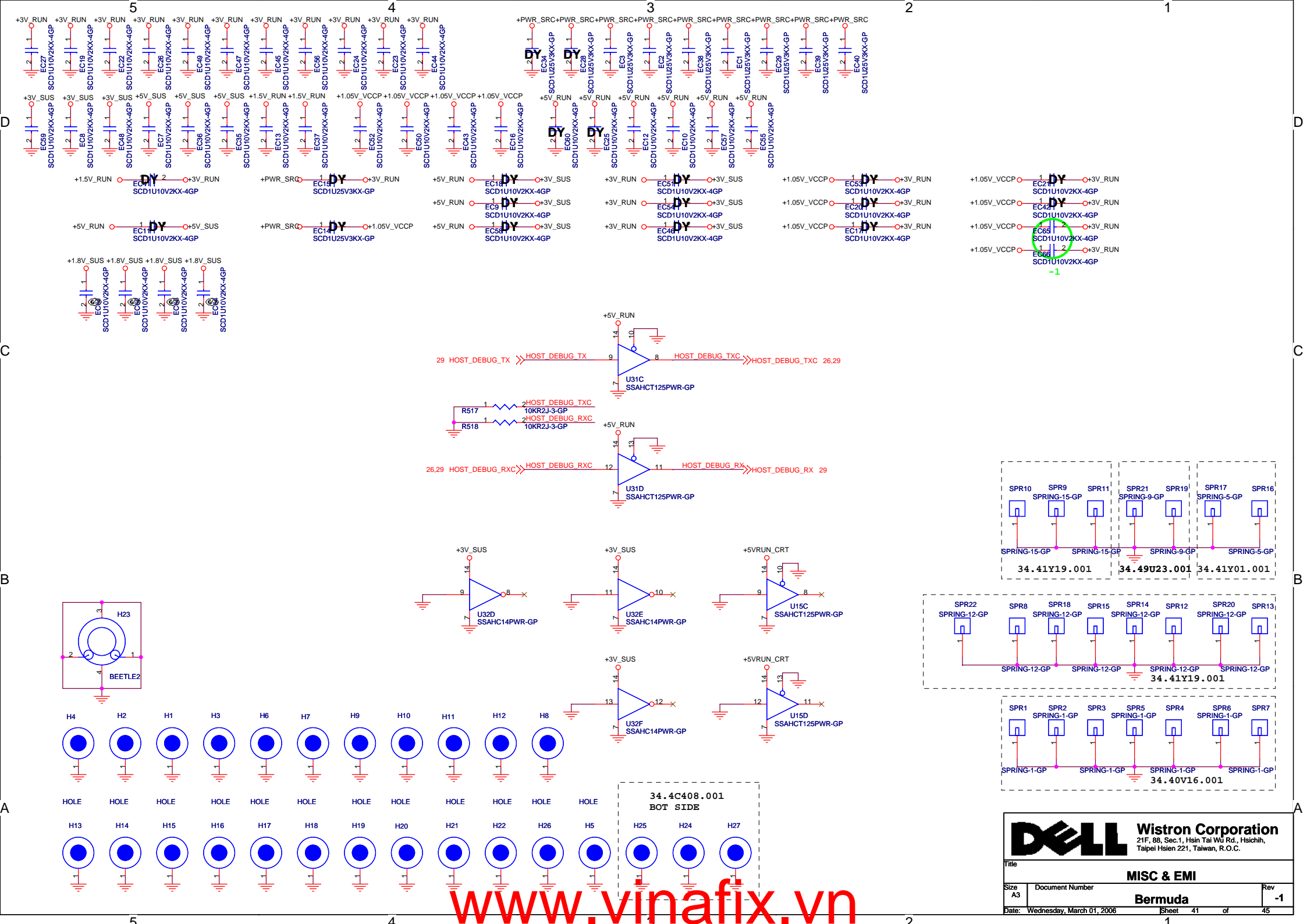


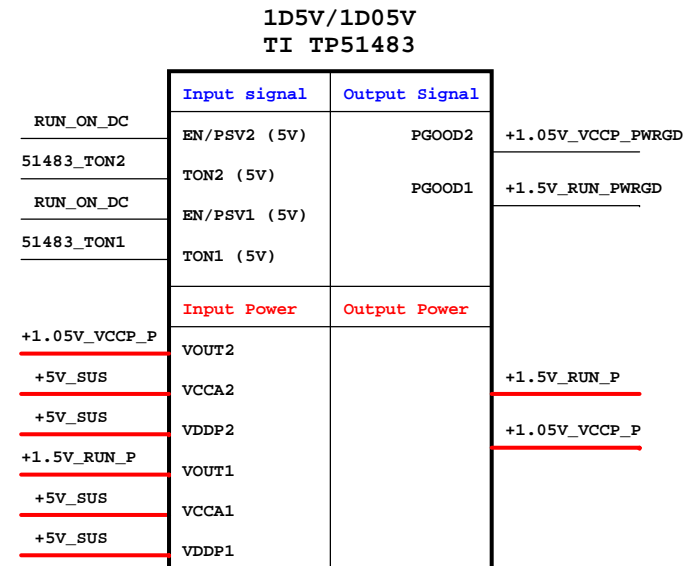
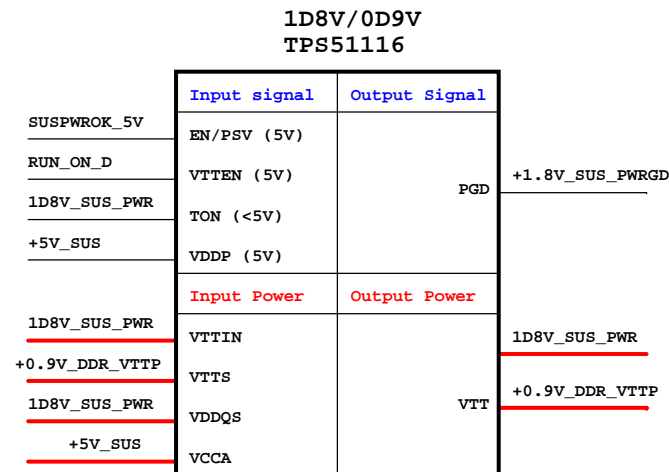
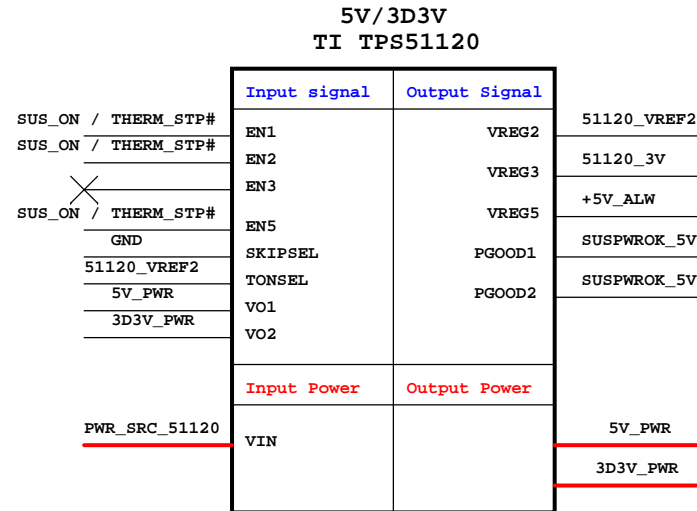
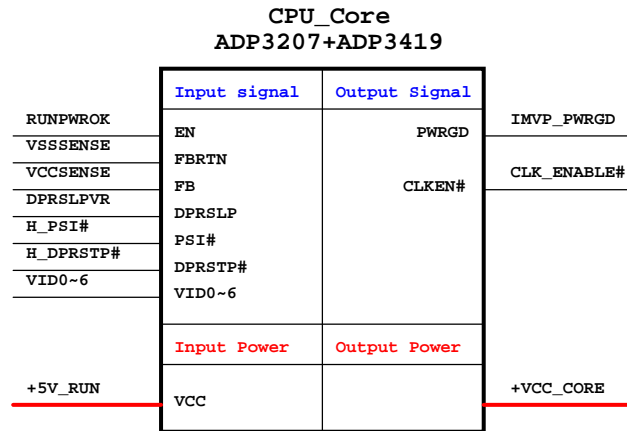
Batt Connector



SC







DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2005/11/03	X00 to X01	1	37	U33 Pin10 change connect from RUN_ON_D to RUN_ON	Follow M07 design	EE
		2	26,29,41	HOST_DEBUG_TX and HOST_DEBUG_RX connect to U31 first then connect to connector(DBG2)	TX,RX need add buffer for debug	EE,SW
		3	8	Del RN40 and add R551,R552(10k ohm) then Pop R440	Implement C4E feature on DPRSLPVR	EE
		4	14,29	Smbus which connect to LCD connector change to SBAT_SMBDAT and SBAT_SMBCLK	This is follow M07 design	EE
		5	15	C112,C113,C121,C129,C139,C155 change from 82p to 0.5p	For TV EA measurement pass	EE
		6	16	R228,R229 change from 33 ohm to 39 ohm	For Azalia EA measurement pass	EE
		7	16	Add R568(0 ohm) for X2(Crystal for ICH7M)	This is follow COE's suggestion	EE
		8	16	C297,C314 change from 4.7P to 3.3P for X2(Crystal for ICH7M)	CRYTAL Vendor suggestion	EE
		9	18	Change R472 to 0805 size and add L48(10UH)	This is follow COE's suggestion	EE
		10	19	Add R560,R561(100k)	Follow M07 design	EE
		11	21,22	Change C250 to 10uF and add C686(0.1u),C687(1u)	This is follow COE's suggestion	EE
		12	23	X1 change from 20p to 18p type crystal	By Broadcom's suggestion,Lan crystal need use 18p type	EE
		13	24	C642,C644 change from 18P to 15P for X5(Crystal for R5C832)	CRYTAL Vendor suggestion	EE
		14	25	Swap connection for CARD1 pin22 and pin23	Card pin22 and pin23 need swap for MS card function work normally	EE
		15	25	Change L29 and L37 to 110 ohm impedance type for 1394	X00 already use 110 ohm type only forget to modify schematic	EE
		16	26	Add D32 and depop R266 to prevent leakage from WAN_RADIO_DIS#	Follow M07 design	EE
		17	27	Change R353 connection from U35 pin1 to U35 pin3	COE's suggestion to prevent the wireless LED light strength not enough	EE
		18	27	R42,R43 change to 220ohm;R40 change to 470ohm	LED light strength need change to avoid light leak	EE
		19	27	Q33 and Q34 Pin1 from +5V_ALW to +3V_ALW	Change to +3VALW for battery LED work normally	EE
		20	29	RN4 and RN6 change from 8.2K to 1K and add R323,R324,R333,R334,C682,C683,C684,C686	For SMBUS EA measurement pass	EE
		21	29	C538,C544 change from 20P to 27P for X4(Crystal for MEC5004)	CRYTAL Vendor suggestion	EE
		22	29	Reversed R553,R554,R555,R556,R557,Q72,Q73,D31,C680,R560	KBC Work Around Circuit for MEC5004 Rev "C"	EE
		23	29	Add R559(0 ohm) to GND	To Fix Rev "C" KBC bug	EE
		24	30	Pop R244 and depop R225	Change BOARD ID to X01	EE
		25	32	Add R562(0 ohm) in EMC4000 pin 22	Easily debug for THERM_STP# signal	EE
		26	33	R321,R330 from 20K ohm to 4K7 ohm R331,R332 from 10K ohm to 200K ohm	To prevent leakage from +3V_SUS to +3V_RUN when in suspend	EE
		27	33	Pop R28,R335,Q6,Q13	For 1.8V_SUS discharge more quickly	EE
		28	33	Change R19 to 200k and C84 to 470pF	For IMVP_PWRGD glitch issue,need make +5V_RUN more faster than +3V_RUN when boot up	EE
		29	33	REMOVE Q8,Q15,R323,R324,R333,R334	Follow M07 design	EE
		30	35	Change R394 to 165K and R396,R397,R401 to 137K then depop C457	This is changed for Vcore load line test fail	Power
		31	35	Change R410,R454 and R165 to 1.5 ohm	This is changed for Vcore's ring over spec	Power
		32	36	Add R565 and R566 for SUS_ON unstable when plug adapter	This is recommended by TDC Lawrence	Power
		33	36	Change TC3 to another source	This is recommended by power team	Power
		34	37	Depop TC18 and change TC17 to 330uF;change D20 to BAT54;change R3 to 13K3 ohm;change R298 to 3D3 ohm	This is recommended by power team	Power
		35	37	New add 4 gaps G75,G76,G77,G78 for 1.8V	This is requested by EMI	EMI
		36	38	Change R427 to 15K4 ohm	This is recommended by power team	Power
		37	39	Add R558,C682 in U5 pin15 pin16 for PBATT_SENSE	To prevent Charger damage when plug battery	Power
		38	39	ADD ADAPT_TRIP_SEL circuit	Follow M07 schematic	Power
		39	41	Add EC61,EC62,EC63,EC64,SPR22 and depop EC41,EC11,EC15,EC14,EC9,EC18,EC58,EC46,EC51,EC54,EC17,EC20,EC53,EC21,EC42	This is for EMI	EMI

